SESSION 9 – TAPA II
High Speed Memory Technology

Wednesday, June 14, 8:30 a.m.
Chairpersons: C. Dennison, Ovonyx Technologies, Inc.
H. Oyamatsu, Toshiba

9.1 – 8:30 a.m.
122 Mb High Speed SRAM Cell with 25nm Gate Length Multi-Bridge-Channel MOSFET (MBCFET) on Bulk Si Substrate, M.S. Kim, S.-Y. Lee, E.-J. Yoon, S.M. Kim, J. Lian, K.-H. Lee, N.M. Cho, M.-S. Lee, D. Hwang, Y.-S. Lee, D.-W. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Kyoungi-Do, Korea

9.2 – 8:55 a.m.
Embedded Bulk FinFET SRAM Cell Technology with Planar FET Peripheral Circuit for *hp*32 nm Node and Beyond, H. Kawasaki, K. Okano, A. Kaneko, A. Yagishita, T. Izumida, T. Kanemura, K. Kasai, T. Ishida, T. Sasaki, Y. Takeyama, N. Aoki, N. Ohtsuka, K. Suguro, K. Eguchi, Y. Tsunashima, S. Inaba, K. Ishimaru, H. Ishiuchi, Toshiba Corporation Semiconductor Company, Yokohama, Japan

Integration schemes of bulk FinFET SRAM cell with bulk planar FET peripheral circuit are studied. Two types of SRAM cells with different beta ratio were investigated in view of static noise margin (SNM). SNM of 122 mV is obtained in the cell with Wfin=15nm, Hfni=90nm , and Lg=20nm at Vdd = 0.6 V. A higher beta ratio (beta ratio> 2.0) in FinFET SRAM is achieved by tuning Hfin of each FinFETs without area penalty.

9.3 – 9:20 a.m.
TiN/HfSiO$_x$ Gate Stack Multi-Channel Field Effect Transistor (McFET) for sub 55nm SRAM Application, S.M. Kim, E.J. Yoon, M.S. Kim, S.D. Suk, M. Li, L. Jun, C.W. Oh, K.H. Yeo, S.H. Kim, S.Y. Lee, Y.L. Choi, N.-Y. Kim, Y.-Y. Yeoh, H.-B. Park, C.S. Kim, H.-M. Kim, D.-C. Kim, H.S. Park, H.D. Kim, Y.M. Lee, D.-W. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Kyoungi-Do, Korea

For the first time, titanium-nitride (TiN) single metal gate and high-k hafnium-silicate (HfSiO$_x$) gate dielectric have been successfully integrated in 55nm McFET SRAM cell. The use of HfSiO$_x$ gate dielectric, not only reduces gate leakage current but also improves ION/IOFF ratio of PFET to 108. Using local fin implantation (LFI) scheme, junction capacitance is reduced by 13% and junction breakdown voltage is increased by 1.4V.

9.4 – 9:45 a.m.
Highly Reliable and Scalable Tungsten Polymetal Gate Process for Memory Devices Using Low-Temperature Plasma Selective Gate Reoxidation, K.-Y. Lim, M.-G. Sung, H.-J. Cho, Y.S. Kim, S.-A. Jang, J.-G. Oh, S.R. Lee, K. Kim, P.-S. Lee, Y.-S. Chun, H.-S. Yang, N.-J. Kwak, H.-C. Sohn, J.-W. Kim, S.-W. Park, Hynix Semiconductor Inc., Kyoungki-Do, Korea

We applied a very low-temperature plasma-type selective gate reoxidation process to W/poly-Si gate for suppression of abnormal oxidation of a low contact resistive WSix/WN diffusion barrier. The device with the plasma selective gate reoxidation showed superior gate oxide reliability and improved stress immunity of transistor compared to the thermally selective gate reoxidized devices.