SESSION 10 – TAPA III
Multi-Standard RF

Thursday, June 19, 10:25 a.m.
Chairpersons: J. Dawson, Massachusetts Institute of Technology
S. Mutoh, NTT Corporation

10.1 – 10:25 a.m.
A Wideband Supply Modulator for 20MHz RF Bandwidth Polar PAs in 65nm CMOS, R. Shrestha, R. van der Zee, A. de Graauw*, B. Nauta, University of Twente, *NXP, The Netherlands

A wideband modulator for a 20MHz bandwidth polar modulated PA is presented which achieves a maximum efficiency of 87.5% and a small signal -3dB bandwidth of 285MHz. Realized in 65nm CMOS, it consists of a cascoded nested Miller compensated linear amplifier and a class D switching amplifier. It can deliver 22.7dBm output power to a 5.3W load. With a switching frequency of 118MHz, the output switching ripple is 4.3mVrms.

10.2 – 10:50 a.m.
A Multi-Mode Multi-band CMOS Direct-Conversion Mobile-TV Tuner for DVB-H/T and T-DMB/DAB Applications, M.-W. Hwang, M. Ahn, S. Beck, J.-C. Lee, S. Hong, S. Lee, S. Jeong, S. Lim, H. Cho, Y.-J. Kim*, I.-C. Hwang**, J. Kim, Future Communications IC Inc., *Korea Acrospace University, **Kangwon National University, Korea

A fully integrated direct-conversion mobile-TV tuner for DVB-H/T and T-DMB/DAB applications was fabricated using 0.18μm CMOS process. This tuner has the good SNR and immunity performance over wide dynamic range for multi-band and multi-mode applications with the automatic gain control and calibration schemes. The power consumption is 127mW for VHF and UHF, and 135mW for L-band at 1.8V supply voltage.

10.3 – 11:15 a.m.
A Quad Band WCDMA Transceiver with Fractional Local Divider, H. Kamizuma, T. Yamawaki, Y. Akamine, K. Maeda, S. Tanaka, K. Hikasa*, Hitachi Central Research Laboratory, *Renesas Technology

We developed a quad band (1, 6, 9, and 11) WCDMA transceiver with digital interface. The developed transceiver uses a 2/5 divider in the local part of the direct conversion architecture. Using the 2/5 divider, reduces the number of local synthesizers to only one in the architecture and avoid VCO pulling phenomena of the local synthesizer perfectly. This transceiver achieved 3% EVM and -46 dB ACLR, which is enough of a margin for standard specifications.

10.4 – 11:40 a.m.
All-Digital Out-phasing Modulator for a Software-Defined Transmitter, M. Heidari, M. Lee, A. Abidi, University of California, Los Angeles, USA

An all-digital out-phasing transmitter suitable for software-defined radio (SDR) is presented. It uses a phase-locked loop followed by two digital phase rotator blocks embedded in two delay-locked loops. The chip is fabricated in a 90nm CMOS process with total active area of 3mm2, and tested for GSM and WCDMA standards. The whole transmitter excluding phase-to-digital converter (PDC) consumes 55mA, and the current consumption of the PDC is 70mA.