SESSION 11 – TAPA II
Processors for HDTV

Thursday, June 19, 1:30 p.m.
Chairpersons: B. Nikolic, University of California, Berkeley
H. Kabuo, Matsushita Electric Ind. Co., Ltd.

11.1 – 1:30 p.m.
A 256mW Full-HD H.264 High-Profile CODEC Featuring Dual Macroblock-Pipeline Architecture in 65nm CMOS, K. Iwata, S. Mochizuki, T. Shibayama, F. Izuhara, H. Ueda, K. Hosogi*, H. Nakata*, M. Ehama*, T. Kengaku, T. Nakazawa, H. Watanabe, Renesas Technology Corp., *Hitachi Ltd., Japan

A video-size-scalable H.264 High-Profile CODEC including 19 specific CPUs for extensibility to multiple standards has been fabricated in 65nm CMOS. With two parallel pipelines for macroblock processing, the CODEC consumed 256mW in real-time encoding of full-HD (1080i) video at an operating frequency of 162MHz. It represents a 38% reduction in power consumption per pixel compared with state-of-the-art designs.

11.2 – 1:55 p.m.
An H.264/AVC Scalable Extension and High Profile HDTV 1080p Encoder Chip, Y.-H. Chen, T.-D. Chuang, Y.-J. Chen, C.-T. Li, C.-J. Hsu*, S.-Y. Chien, L.-G. Chen, National Taiwan University, *UMC, Taiwan

The first single-chip H.264/AVC HDTV 1080p encoder for scalable extension (SVC) with high profile is implemented on a 16.76mm2 die with 90nm process. It dissipates 349/439mW at 120/166MHz for high profile and SVC encoding. The proposed frame-parallel architecture halves external memory bandwidth and operating frequency. Moreover, the prediction architecture with inter-layer prediction tools are applied to further save 70% external memory bandwidth and 50% internal memory access.

11.3 – 2:20 p.m.
An H.264/AVC High422 Profile and MPEG-2 422 Profile Encoder LSI for HDTV Broadcasting Infrastructures, K. Nitta, M. Ikeda, H. Iwasaki, T. Onishi, T. Sano, A. Sagata, Y. Nakajima, M. Inamori, T. Yoshitome, H. Matsuda, R. Tanida, A. Shimizu, J. Naganuma, K. Nakamura, Nippon Telegraph and Telephone Corporation, Japan

An H.264/AVC High422 profile encoder LSI has been developed for HDTV broadcasting infrastructures. It contains 257GOPS ME/MC engines with search ranges of -271.75 to +199.75 (H), -109.75 to +145.75 (V), that support almost all H.264/AVC ME/MC tools. Our evaluations show that it can encode fast moving scenes with 1.2 to 1.7dB higher than the JM. It was successfully fabricated in a 90nm 9level metal CMOS technology with 140 million transistors.

11.4 – 2:45 p.m.
A 2/4/8 Antennas Configurable Diversity OFDM Receiver For Mobile HDTV Application, T. Wada, T. Iida**, H. Mizutani*, S. Sakaguchi*, S. Murakami*, A. Shimizu**, University of the Ryukyus, *Magna Design Net, Inc., **Sanyo Electric Co., Japan

Two array antennas and one carrier diversity combiners are integrated with Japan Terrestrial digital TV (ISDB-T) OFDM receiver using 90nm 7M1P CMOS process. A 2/4/8 antennas diversity receiver can be configured and the low cost 4 antennas diversity reception system can be realized by one LSI. The mobile reception performance is increase by 63% using de-noise filter circuit and SPLINE interpolator. The die area is 49mm2 and the power consumption is 310mW.