SESSION 12 – TAPA III
PLLs and Wireless Transceivers

Thursday, June 19, 1:30 p.m.
Chairpersons: C.-M. Hung, Texas Instruments
M. Ikeda, University of Tokyo

12.1 – 1:30 p.m.
A Low Noise, Wideband Digital Phase-Locked Loop Based On A New Time-To-Digital Converter With Subpicosecond Resolution, M. Lee, M. Heidari, A. Abidi, University of California, Los Angeles, USA

A digital PLL uses a high resolution coarse-fine Time-to-Digital Converter (TDC) for wide loop bandwidth. The loop bandwidth is set to 400 kHz with a 26 MHz reference for GSM. The in-band phase noise contribution from the TDC is -116 dBc/Hz, the phase noise is -117 dBc/Hz at high-band 400 kHz offset, and the RMS phase error is 0.3°.

12.2 – 1:55 p.m.
A 0.4ps-RMS-Jitter 1-3GHz Ring-Oscillator PLL using Phase-Noise Preamplification, Z. Cao, Y. Li*, S. Yan, University of Texas at Austin, *Analog Devices, USA

A 1-3GHz tunable multiply-by-8 PLL is implemented in 0.13μm CMOS and occupies 0.07mm2. A proposed fully-differential Gm-C loop filter structure decouples reference spur performance from charge-pump current matching and loop filter leakage, while enables phase error preamplification to lower PLL in-band noise without reducing VCO analog tuning range or increasing loop filter capacitor size. It achieves <-118dBc/Hz PLL in-band noise (>100kHz offset) and 0.4ps-rms jitter (integrated from 3kHz to 300MHz offset) for ≥2.5GHz outputs.

12.3 – 2:20 p.m.
RF Transceiver and Wireless Calibration of On-Chip Frequency Reference for a True Single Chip Radio, Y. Ding, Y. Su, C. Cao, J.-J. Lin, T. Wu, M. Hwang, R. Fox, J. Brewer, K. O, University of Florida, USA

An RF transceiver for operation near 24GHz with an onchip antenna, fractional-N synthesizer and other RF and analog baseband circuits is demonstrated in 130-nm CMOS. A 5-m wireless link was demonstrated using a transceiver pair. A technique for wireless calibration of an on-chip frequency reference is also demonstrated.

12.4 – 2:45 p.m.
A 100Mbps, 0.41mW, DC-960MHz Band Impulse UWB Transceiver in 90nm CMOS, L. Liu, Y. Miyamoto, Z. Zhou, K. Sakaida, R. Jisun, K. Ishida, M. Takamiya, T. Sakurai, University of Tokyo, Japan

A low power impulse ultra-wideband (UWB) transceiver for DC-960MHz band is proposed in this paper. It features a digital pulse-shaping transmitter, a DC power-free pulse discriminator and an error-recovery phase-frequency detector. The developed transceiver in 90nm CMOS achieves the lowest energy consumption of 2.2pJ/bit (TX) and 1.9pJ/bit (RX) at 100Mbps.