SESSION 14 – TAPA III
Power Management Circuits and Image Sensor

Thursday, June 19, 3:25 p.m.
Chairpersons: T. Kwan, Broadcom Corp.
M. Igarashi, Sony Corp.

14.1 – 3:25 p.m.
Single-Inductor Dual-Output DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices, M.-H. Huang, K.-H. Chen, W.-H. Wei*, National Chiao Tung University, *Richtek Technology Corp., Taiwan

A peak-current control single-inductor dual-output (SIDO) DC-DC converter is proposed. The proposed SIDO DC-DC converter not only provides dual output sources (one buck and one boost outputs) but also has minimized cross regulation. Besides, a new hysteresis mode decided by a power decision circuit can effectively prevent SIDO converter from oscillating when power of buck is larger than that of boost. SIDO converter achieves high conversion efficiency at light loads. Experimental results show a high efficiency from 85% at light loads to 94% at heavy loads.

14.2 – 3:50 p.m.
Adaptive Step-Down Switched-Capacitor Power Converter with *z*-Domain Observation-Based Line-Load Regulation, M. Song, I. Chowdhury, D. Ma, A.P. Brokaw*, University of Arizona, *Analog Devices, USA

The paper presents an integrated switched-capacitor power converter, employing an efficient step-down conversion power stage and a cost-effective observation-based controller. The complete z-domain design makes system modeling and analysis consistent and efficient. With an adjustable output voltage range from 1.25 to 2.0V, the converter delivers up to 220mW power from a 3.3 V input source with a maximum efficiency of 74.1%, surpassing a linear regulator's theoretical limit.

14.3 – 4:15 p.m.
An SC Voltage Regulator with Novel Area-Efficient Continuous Output Regulation by Dual-Branch Interleaving Control Scheme, F. Su, W.-H. Ki, C.-Y. Tsui, Hong Kong University of Science and Technology, Hong Kong

A 1.8V to 3.3V SC voltage regulator is present. The dual branches operate in an interleaving fashion for sake of area-efficient continuous output regulation. Therefore the output voltage can be continuously regulated with small ripples. The design was fabricated in 0.35μm CMOS process. A maximum output ripple of 10mV is maintained for loading from 10mA to 180mA. Meanwhile load regulation of 0.0043%/mA and load transient of less than 25us for 150mA current step are measured.

14.4 – 4:40 p.m.
A Very Low Column FPN and Row Temporal Noise 8.9M-Pixel, 60 fps CMOS Image Sensor with 14bit Column Parallel SA-ADC, S. Matsuo, T. Bales, M. Shoda, S. Osawa, B. Almond*, Y. Mo**, J. Gleason**, T. Chow**, I. Takayanagi, Micron Japan Ltd., Japan, *Micron Europe, United Kingdom, **Micron Technology, USA

A 1.25-inch optical format, 8.9M-pixel CMOS image sensor that employs a 4T pinned photodiode (P-PD) pixel and 14bit column ADCs is reported. A 14bit or 12bit digital video signal is streamed out via 16-lane low-voltage, low-power differential serial output ports in 50fps and 60fps operations, respectively. Temporal noise floor of 2.8e-rms and linear full-well of 27.8ke- were obtained at 60 fps operation. Row temporal noise and column FPN are as small as 0.31 e-rms and 0.36 e-rms, respectively.