SESSION 15 – TAPA I
Power-Aware Circuit Techniques

Friday, June 20, 8:15 a.m.
Chairpersons: J. Barth, IBM Microelectronics
T. Shiota, Fujitsu Laboratories, Ltd.

15.1 – 8:15 a.m.
A Sub-µs Wake-up Time Power Gating Technique with Bypass Power Line for Rush Current Support, K. Kawasaki, T. Shiota, K. Nakayama, A. Inoue, Fujitsu Laboratories Ltd., Japan

A sub-us wake-up power gating technique was developed for low power SOCs. It uses two types of power switches and separated power lines bypassing rush current to suppress power supply voltage fluctuations. We applied this technique to a heterogeneous dual-core microprocessor fabricated in 90nm CMOS technology. When wake-up time on the 2M-gate scale circuit was set to 0.24us, the supply voltage fluctuation was suppressed to 2.5mV.

15.2 – 8:40 a.m.
Dynamic Voltage Boost (DVB) Method for Improving Power Integrity of Low-Power Multi-Processor SoCs, Y. Kanno, K. Yoshizumi, Y. Yasu, K. Ishibashi, H. Mizuno, Hitachi Ltd., Japan

We propose a dynamic voltage boosting (DVB) method for improving performance by slightly boosting voltage within a withstand voltage. We measured an improvement of 44 % voltage drop with about 10 % area overhead in a 65 nm CMOS. This DVB method combined with a series power gating can be used to achieve high performance for low-cost low-power SoCs in advanced process technology.

15.3 – 9:05 a.m.
Experimental Evaluation of Digital-Circuit Susceptibility to Voltage Variation in Dynamic Frequency Scaling, M. Fukazawa, M. Kurimoto**, R. Akiyama*, H. Takata**, M. Nagata, Kobe University, *Renesas Technology Corp., ** Renesas Design, Japan

Logical operations in CMOS digital integration are highly prone to fail as the amount of power-supply (PS) drop approaches to threshold. PS voltage variation is characterized by built-in noise monitors in a 32-bit microprocessor of 90-nm CMOS technology, in relation with instruction-level programming for logical failure analysis. Experimental measurements demonstrate that the increased susceptibility of processor operation with dynamic frequency scaling (DFS) can be mitigated through PS noise shaping.

15.4 – 9:30 a.m.
A 1.1V 35µm × 35µm Thermal Sensor With Supply Voltage Sensitivity Of 2ºC/10%-Supply For Thermal Management On The SX-9 Supercomputer, E. Saneyoshi, K. Nose, M. Kajita, M. Mizuno, NEC Corporation, Japan

Presented here is a thermal sensor, based on transistor off-leakage current, that allows measurement error of less than 3.1ºC at 90ºC and less than 2ºC at 10% Vdd deviation. For experimental evaluation, 11 thermal sensors, each of which occupied only 35µm × 35µm area, were placed on a chip, and both the location of a hotspot and the overall temperature distribution were successfully measured and agreed with simulation.