SESSION 16 – TAPA II
60-120GHz Wireless Receivers

Friday, June 20, 8:15 a.m.
Chairpersons: F. Dai, Auburn University
K. Agawa, Toshiba

16.1 – 8:15 a.m.
A 1Gbps Mixed-Signal Analog Front End for a 60GHz Wireless Receiver, D.A. Sobel, R.W. Brodersen, University of California, Berkeley, USA

A low-power, mixed-signal, baseband analog front end for 60GHz 1Gb/s wireless communications has been implemented in a standard 90nm CMOS process. The receiver is capable of operating under indoor multipath scenarios, resolving channels with up to 32ns multipath delay spread. It uses mixed-signal equalization and carrier recovery in order to minimize the dynamic range requirements of the converter circuitry, resulting in a low power consumption of 55mW.

16.2 – 8:40 a.m.
19.2mW 2Gbps CMOS Pulse Receiver for 60GHz Wireless Communication, A. Oncu, M. Fujishima, University of Tokyo, Japan

A low-power 60GHz pulse receiver has been fabricated for over-Gbps wireless communication by a standard 90nm CMOS process. The receiver consists of a nonlinear detecting amplifier, a limiting amplifier, an offset canceller and a buffer. The measured sensitivity is the average power of -20dBm for millimeter-wave pulses of 60GHz. The power dissipation and maximum data rate of the receiver are 19.2mW and 2Gbps, respectively. These results indicate the possibility of new low-power and ultrahigh-speed wireless communication using millimeter-wave pulses with CMOS implementation.

16.3 – 9:05 a.m.
A Dual-band 61.4~63GHz/75.5~77.5GHz CMOS Receiver in a 90nm Technology, K.-H. Chen, C. Lee, S.-I. Liu, National Taiwan University, Taiwan

A dual-band 61.4~63GHz/75.5~77.5GHz receiver has been realized in a 90nm CMOS technology. It is composed of a broadband low-noise amplifier, RF/IF mixers, and a quadruplicate-locked phase-locked loop. With the dual down- conversion approach, this dual-band receiver achieves a conversion voltage gain of 25.2dB at 62.5GHz and 19.4dB at 77GHz with an input P1dB of -16dBm. It consumes 132mW from a 1.5V supply.

16.4 – 9:30 a.m.
Circuit Performance Characterization of Digital 45-nm CMOS Technology for Applications around 110GHz, R.A. Aroca, A. Tomkins, Y. Doi*, T. Yamamoto*, S.P. Voinigescu, University of Toronto, Canada, *Fujitsu Laboratories Ltd., Japan

The first 50-GHz to 110-GHz downconverter in 45-nm digital CMOS is presented along with the mm-wave characterization of AMOS varactors, inductors, and transformers. The varactor Q is higher than 6, up to 94 GHz. The downconverter gain is 15dB at 111GHz, and is employed as a broadband test vehicle to characterize the optimal noise figure current density (JOPT) of 45-nm MOSFETs in the 50 GHz to 110 GHz range.