Friday, June 20, 3:25 p.m.
Chairpersons: G. Lehmann, Infineon Technologies
C. Kim, Samsung Electronics Co., Ltd.

21.1 – 3:25 p.m.
A One MB Cache Subsystem Prototype with 2GHz Embedded DRAMs in 45nm SOI CMOS, P. Klim, J. Barth, W. Reohr*, D. Dick, G. Fredeman, G. Koch, H. Le, A. Khargonekar, P. Wilcox, J. Golz, J.B. Kuang*, A. Mathews, T. Luong, H. Ngo, R. Freese**, H. Hunter*, E. Nelson, P. Parries, T. Kirihata, S. Iyer, IBM Systems and Technology Group, *IBM Research Division, **Advanced Micro Devices, USA

We present a 1MB cache subsystem that integrates 2GHz embedded DRAM macros, charge pump circuits, a 4Kb one-time-programmable ROM, clock multipliers, and built-in self test circuitry, having a 36.5GB/s peak system data-rate. The eDRAM employs a programmable pipeline, achieving a 1.8ns latency.

21.2 – 3:50 p.m.
A High Performance 2.4 Mb L1 and L2 Cache Compatible 45nm SRAM with Yield Improvement Capabilities, R. Joshi, R. Houle, D. Rodko, P. Patel, W. Huott, R. Franch, Y. Chan, D. Plass, S. Wilson, S. Wu, R. Kanj, IBM, USA

A fully functional and stable 2.4 Mb L1 and L2 Cache compatible 6T SRAM is demonstrated. Measured results show operation from -40oC to 120oC, speed of 6.5 GHz and 3.8 GHz for L1-Cache cells and L2-Cache cells, respectively, at 1 V and 25oC, with high yield. Key features include multi-setting programmable clock block, separate read/write margin circuitry, low noise dynamic decoders, bit select circuitry supported by newly developed fast Monte Carlo technique.

21.3 – 4:15 p.m.
A 0.6V 45nm Adaptive Dual-rail SRAM Compiler Circuit Design for Lower VDD_min VLSIs, Y.H. Chen, W.M. Chan, S.Y. Chou, H.J. Liao, H.Y. Pan, J.J. Wu, C.H. Lee, S.M. Yang, Y.C. Liu, H. Yamauchi*, TSMC, Taiwan, *Fukuoka Institute of Technology, Japan

A 0.6V 45nm dual-rail SRAM design utilizing an adaptive voltage regulator targeting for an SRAM compiler application is proposed for the first time. To relax IR-drop constraints of CVDD power routings in P&R flow, shifting bite-line (BL) pre-charge power supply from CVDD to VDD is adopted in this work. This also avoids the congestion of the VDD and CVDD power mesh. A 45nm test chip has demonstrated that these concepts successfully can push the VDD_min down to 0.6V, which is > 250mV lower than the conventional single-rail SRAM's.

21.4 – 4:40 p.m.
A 45-nm Single-port and Dual-port SRAM Family with Robust Read/Write Stabilizing Circuitry under DVFS Environment, K. Nii, M. Yabuuchi, Y. Tsukamoto, S. Ohbayashi, Y. Oda*, K. Usui**, T. Kawamura, N. Tsuboi, T. Iwasaki, K. Hashimoto, H. Makino, H. Shinohara, Renesas Technology Corporation, *Shikino High-Tech Corporation, **Daioh Electric Corporation, Japan

We propose an enhanced design solution for embedded SRAM macros under DVFS environment. The improved wordline suppression technique compensates the read stability against process variation, facilitating the Fab. portability. The negative bitline technique expands the write margin for not only 6T single-port (SP) cell but also 8T dual-port (DP) cell even at the 0.7V lower supply voltage. Using 45-nm CMOS technology, we fabricated both SP and DP SRAMs with the proposed circuitry. We achieve robust operations from 0.7V to 1.3V wide supply voltage.