Friday, June 20, 3:25 p.m.
Chairpersons: K. Gulati, Cambridge Analog Technologies Inc.
M. Nagata, Kobe University

22.1 – 3:25 p.m.
A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Residue Amplification, J. Hu, N. Dolev, B. Murmann, Stanford University, USA

An ultra-low power pipelined ADC is realized by replacing conventional op-amp circuits with dynamic source-follower gain stages. The presented 90-nm CMOS converter operates at 50MS/s and achieves an SNDR of 49.4dB while dissipating 1.44mW from a 1.2-V supply.

22.2 – 3:50 p.m.
A Fully-Differential Zero-Crossing-Based 1.2V 10b 26MS/s Pipelined ADC in 65nm CMOS, S.-K. Shin, Y.-S. You, S.-H. Lee, K.-H. Moon, J.-W. Kim, L. Brooks*, H.-S. Lee*[1,*2], Samsung Electronics, Korea, *[1]Massachusetts Institute of Technology, USA, *[2]Cambridge Analog Technologies, Inc., USA

A fully-differential zero-crossing-based 10b 26MS/s pipelined ADC in a 65 nm CMOS process is presented. Switched-capacitor overshoot correction is compatible with the differential topology and allows faster operation. A CMFB is engaged in the coarse phase for constant common-mode. The 0.33mm2 ADC achieves 54.3dB SNDR with a FOM of 161fJ/step.

22.3 – 4:15 p.m.
A 12b 50MS/s 10.2mA 0.18µm CMOS Nyquist ADC with a Fully Differential Class-AB Switched OP-AMP, H.-C. Choi, Y.-J. Kim, M.-H. Lee, Y.-L. Kim, S.-H. Lee, Sogang University, Korea

A 12b 50MS/s pipelined ADC based on a fully differential class-AB switched op-amp achieves low power consumption with a high differential input range of 2.4Vp-p. The proposed input sampling network samples wideband signals exceeding the Nyquist frequency without a SHA. The prototype ADC in a 0.18µm CMOS shows a power dissipation of 18.4mW at 50MS/s and 1.8V with an active die area of 0.26mm2.

22.4 – 4:40 p.m.
A Process-Scalable Low-Power Charge-Domain 13-bit Pipeline ADC, M. Anthony, E. Kohler, J. Kurtze, L. Kushner, G. Sollner, Kenet Inc., USA

A 13-bit ADC is implemented using a novel charge-domain architecture. Enhanced bucket-brigade circuitry and a tapered charge pipeline provide precision charge-domain operation in a standard CMOS process, while eliminating the need for signal-path op-amps. The prototype ADC, implemented in 0.18µm CMOS, provides 10.65 ENOB at 250 MS/s while consuming only 140 mW, yielding an exceptionally low FoM of 0.28 pJ/conversion-step. Simulations indicate that the architecture and circuitry are well suited to scaling below 90nm.