SESSION 3 – TAPA II
Parallel Processing

Wednesday, June 18, 1:30 p.m.
Chairpersons: J. Farrell, AMD
K. Kobayashi, Kyoto University

3.1 – 1:30 p.m.
A 167-processor 65 nm Computational Platform with Per-Processor Dynamic Supply Voltage and Dynamic Clock Frequency Scaling, D. Truong, W. Cheng, T. Mohsenin, Z. Yu, T. Jacobson, G. Landge, M. Meeuwsen, C. Watnik, P. Mejia, A. Tran, J. Webb, E. Work, Z. Xiao, B. Baas, University of California, Davis, USA

A 167-processor 65 nm computational platform well suited for DSP, communication, and multimedia workloads contains 164 programmable processors with dynamic supply voltage and dynamic clock frequency circuits, 3 algorithm-specific processors, and 3 16 KB shared memories, all clocked by independent oscillators and connected by configurable long-distance-capable links.

3.2 – 1:55 p.m.
A 26mW 6.4GFLOPS Multi-Core Stream Processor for Mobile Multimedia Applications, Y.-M. Tsao, C.-H. Sun, Y.-C. Lin, K.-H. Lok, C.-J. Hsu*, S.-Y. Chien, L.-G. Chen, National Taiwan University, Taiwan, *UMC, Taiwan

A 26mW 6.4GFLOPS multi-core stream processor for mobile applications is implemented in 90nm CMOS technology. A unified stream processing architecture with power-aware frequency scaling and adaptive task scheduling techniques are proposed to reduce the power consumption and increase the performance to achieve the performance of 200Mvertices/s and 400Mpixels/s in 3D graphic applications.

3.3 – 2:20 p.m
The Brain Mimicking Visual Attention Engine: An 80x60 Digital Cellular Neural Network for Rapid Global Feature Extraction, S. Lee, K. Kim, M. Kim, J.-Y. Kim, H.-J. Yoo, KAIST, Korea

The Visual Attention Engine(VAE), an 80x60 digital Cellular Neural Network, rapidly extracts global features used as attentional cues to streamline detailed object recognition. A peak performance of 24GOPS is achieved by 120 processing elements (PE) shared by the cells. 2D Shift register based data transactions enable 93% PE utilization. Integrated within an object recognition SoC, the 4.5mm2 VAE running at 200MHz improves object recognition frame rate by 83% while consuming just 84mW.

3.4 – 2:45 p.m.
A 100 GOPS In-vehicle Vision Processor for Pre-crash Safety Systems Based on a Ring Connected 128 4-Way VLIW Processing Elements, S. Kyo, S. Okazaki, T. Koga*, F. Hidano*, NEC Corporation, Japan, *NEC Electronics Corporation, Japan

A 100GOPS vision processor LSI (IMAPCAR) for in-vehicle image recognition which consumes less than 2 watts of power has been developed. 128 of 4-Way VLIW with MAC (multiply add accumulation) processor elements (PE) to which data are assigned efficiently by DMA companion scaling capability, has achieved high performance in low cost. Compared with a previous design, performance for major vision tasks has been improved by a factor of 2.5 while 50% of power is reduced.