SESSION 4 – TAPA III
Low-Power and Reconfigurable RF

Wednesday, June 18, 1:30 p.m.
Chairpersons: A. Abidi, University of California, Los Angeles
H. Ishikuro, Keio University

4.1 – 1:30 p.m.
A 350uW CMOS MSK Transmitter and 400uW OOK Super-Regenerative Receiver for Medical Implant Communications, J.L. Bohorquez, J.L. Dawson, A.P. Chandrakasan, Massachusetts Inst. of Tech, USA

A 350µW MSK direct modulation transmitter and 400µW OOK super-regenerative receiver are implemented in 90nm CMOS technology. The transceiver tunes 24MHz in frequency steps smaller than 2kHz and is optimized for the Medical Implant Communications Service (MICS) standard in the 402--405MHz band. The transmitter meets MICS mask specifications with data rates up to 120kbps, and the receiver has a sensitivity better than -99dBm with a data rate of 40kbps or -93dBm with a data rate of 120kbps.

4.2 – 1:55 p.m.
A 5GHz Fully Integrated Super-regenerative Receiver with On-chip Slot Antenna in 0.13µm CMOS, D. Shi, N. Behdad*, J.-Y. Chen**, M. Flynn, University of Michigan, *University of Central Florida, **ZeroG Wireless Inc., USA

A super-regenerative receiver with a novel on-chip slot antenna and a compact capacitively-loaded standing-wave resonator is reported. An all-digital PLL synchronizes the received data clock. The prototype 5GHz receiver, implemented in 0.13µm CMOS, achieves a highest data rate of 1.2Mb/s, dissipates 6.6mW from a 1.5V supply, and occupies a die area of 2.4mm2

4.3 – 2:20 p.m.
A Direct Conversion Receiver Adopting Balanced Three-phase Analog System, T. Yamaji, T. Itakura, T. Ueno, Toshiba Corporation, Japan

A new wireless receiver architecture that has small analog area is proposed and evaluation of the core analog blocks is described. To reduce the analog area, a balanced 3-phase analog system is adopted and the functions of analog baseband filters and VGAs are moved to digital domain. The downconverter and ADC are directly connected and they occupy 0.28 mm2.

4.4 – 2:45 p.m.
A Direct-Conversion CMOS RF Receiver Reconfigurable from 2GHz to 6GHz, J. Park, S.-N. Kim, J.-H. Seok, Y.-S. Roh, C. Yoo, K. Lim*, J. Kim*, Hanyang University, Korea, *Future Communications IC Inc., Korea

A CMOS direct-conversion receiver with only one signal path is reconfigurable from 2GHz to 6GHz in the RF band and from 3.6MHz to 54MHz in the channel bandwidth. By employing a voltage feedback in a common-gate low-noise amplifier (LNA), the input matching of the LNA can be reconfigured for each RF band by simply changing the resonant frequency of load network. Implemented in a 0.18µm 1P5M RF CMOS technology, the whole receive path shows 4.6~5.6dB noise figure.