SESSION 7 – TAPA II
Clocking and Signaling

Thursday, June 19, 8:30 a.m.
Chairpersons: K. Shepard, Columbia University
K. Nose, NEC Corporation

7.1 – 8:30 a.m.
Next Generation Intel® Micro-architecture (Nehalem) Clocking Architecture, N. Kurd, J. Douglas, P. Mosalikanti, R. Kumar, Intel Corporation, USA

This paper describes the Next generation Intel® micro-architecture (Nehalem) 45nm IA processor's Core and I/O clocking architecture. Among the highlights are: configurable clocking, fast-lock low-skew PLLs, high reference clock frequencies, analog supply tracking system, adaptive frequency clocking, low jitter Intel® QuickPath interconnect and Intel® QuickPath memory controller clock generation, and jitter-attenuating DLLs.

7.2 – 8:55 a.m.
A Small-Delay Defect Detection Technique For Dependable LSIs, K. Noguchi, K. Nose, T. Ono*, M. Mizuno, NEC Corporation, *NEC Electronics Corporation, Japan

As continuous process scaling produces large-scale chips, small-delay defects become one of the major chip-reliability limiters. Small-delay defect detection techniques for LSI screening have been developed, which can successfully detect outlier chips among normally-distributed chips in a short testing time. In our experiments with 90nm CMOS 100MHz test chips, we have successfully detected around 1-ns path delay shift caused by small-delay defects in only 1/25 of testing time.

7.3 – 9:20 a.m.
Sensor Data Retrieval Using Alignment Independent Capacitive Signaling, Y.-S. Lin, D. Sylvester, D. Blaauw, University of Michigan, USA

We propose a capacitive coupling based method for sensor data retrieval which can be easily integrated with miniature sensor nodes of sub-mm scale. An alignment independent mechanism is implemented to achieve <15% difference in achievable data rate when the sensor chip is randomly dropped on the data retrieval chip regardless of alignment. To enable passive operation of the sensor chip, the data retrieval chip send power to/receive signal from the sensor chip simultaneously.

7.4 – 9:45 a.m.
Characterizng Sampling Aperture of Clocked Comparators, M. Jeeradit, J. Kim, B. Leibowitz, P. Nikaeen*, V. Wang**, B. Garlepp^, C. Werner, Rambus Inc., *Stanford University, **University of California, Los Angeles, ^SiTime Corp, USA

Practical simulation and measurement methods based on impulse sensitivity functions to characterize the sampling aperture of clocked comparators are demonstrated on a 90nm CMOS testchip. The results comparing a StrongARM latch and a CML latch suggest that the StrongARM latch has a narrower aperture of 23ps but its aperture center is more sensitive to supply (65ps/V). The CML latch has a higher sampling gain of 88.8dB but a lower bandwidth of 6.8GHz.