SESSION 9 – TAPA II
Frequency Synthesis Components

Thursday, June 19, 10:25 a.m.
Chairpersons: A. Amerasekera, Texas Instruments
J. Lee, National Taiwan University

9.1 – 10:25 a.m.
An Efficient High-Resolution 11-Bit Noise-Shaping Multipath Gated Ring Oscillator TDC, M. Straayer, M. Perrott, Massachusetts Institute of Technology, USA

An 11-bit, 50-Msps time-to-digital converter (TDC) using a multipath gated ring oscillator (GRO) with 6ps of delay per stage achieves low power (2.2 to 21mW) and small area of 160x260µm in 0.13µm CMOS. The structure also achieves first order noise shaping of the GRO quantization and mismatch noise; the resulting TDC error integrates to < 100 fs (rms) in a 1 MHz bandwidth to achieve dynamic range of over 90dB with no calibration required.

9.2 – 10:50 a.m.
Digital Frequency Detector based on Multiphase Ring Oscillator, C.-Y. Cha, M. Lee*, J. Lee, T. Kim, Samsung Advanced Institute of Technology, Korea, *University of California, Los Angeles, USA

A new high resolution digital frequency detector architecture based on multiphase ring oscillator is proposed, and it uses the time resolution of fast-operating deep sub-micron MOS transistor. The proposed DFD is implemented with 65nm CMOS technology. The measured frequency resolution is amount to 75dBc with 10.2MHz input signal. Fabricated digital frequency detector draws about 4mA in 1.2V supply voltage.

9.3 – 11:15 a.m.
93.5~109.4GHz CMOS Injection-Locked Frequency Divider With 15.3% Locking Range, L.-C. Cho, K.-H. Tsai, C.-C. Hung, S.-I. Liu, National Taiwan University, Taiwan

A distributed-LC injection-locked frequency divider is proposed. This frequency divider has been realized in 65nm CMOS technology. The core area is 0.036mm2. The measured operation range is 93.5~109.4GHz. Its center frequency is 102GHz and the locking range is 15.3%. Its power is 5.5mW from the supply of 1.1V.

9.4 – 11:40 a.m.
A 2.5-GHz 860µW Charge-Recycling Fractional-N Frequency Synthesizer in 130nm CMOS, D. Park, W. Lee, S. Jeon, S.H. Cho, KAIST, Korea

A 1.2V 2.5GHz 860µW fractional-N synthesizer is implemented in 130nm CMOS. It employs charge recycling technique for implicit DC-DC conversion without using any voltage regulators, and achieves -77dBc/Hz and -113.5dBc/Hz of phase noise at 100kHz and 1MHz offset, respectively. Self-biased divider and VCO enables robust operation of the proposed circuit.