SPECIAL SESSION – TAPA II
Technology Highlights

Wednesday, June 18, 10:25 a.m.
Chairpersons: C. Dennison, Ovonyx Technologies
M. Niwa, Matsushita Electric Ind. Co.

9.1 - 10:25 a.m.
Fully Integrated and Functioned 44nm DRAM Technology for 1GB DRAM, H. Lee, D.-Y. Kim, B.-H. Choi, G.-S. Cho, S.-W. Chung, W.-S. Kim, M.-S. Chang, Y.-S. Kim, J. Kim, H.-J. Lee, H.-S. Song, S.-K. Park, J.-W. Kim, S.-J. Hong, S.-W. Park, Hynix Semiconductor, Korea

Hynix demonstrates for the first time a fully integrated and functional 1Gb DRAM at 44nm with cell size of only $0.015\mu m^2$. To overcome DRAM scaling challenges: a novel "saddle-fin" access transistor, ZAZ ($ZrO_2/Al_2O_3/ZrO_2$) storage capacitor MIM structure and low resistance W word line are utilized I this fully integrated 1Gb DRAM.

9.2 - 10:50 a.m.
A Cost Effective 32nm High-K/ Metal Gate CMOS Technology for Low Power Applications with Single-Metal/Gate-First Process, X. Chen, S. Samavedam*, V. Narayanan, K. Stein, C. Hobbs*, C. Baiocco, W. Li, D. Jaeger, M. Zaleski*, S. Yang, N. Kim**, Y. Lee, D. Zhang*, L. Kang*, J. Chen**, H. Zhuang^, A. Sheikh, J. Wallner, M. Aquilino, J. Han^, Z. Jin, J. Li, G. Massey, S. Kalpat, R. Jha, N. Moumen, R. Mo, S. Kershnan, Z. Wang, M. Chudzik, M. Chowdhury*, D. Nair, C. Reddy*, Y.W. Teh**, C. Kothandaraman, D. Coolbaugh, S. Pandey**, D. Tekleab**, A. Thean*, M. Sherony, C. Lage*, J. Sudijono**, R. Lindsay^, J.-H. Ku^^, M. Khare, A. Steegen, IBM SDRC, *Freescale Semiconductor, **Chartered Semiconductor Manufacturing, ^Infineon Technologies, ^^Samsung Electronics Co., USA

IBM / Freescale Semiconductor / Charter Semiconductor / Infineon Technologies / Samsung Electronics jointly present for the first time a 32 nm high K / metal gate low power cost effective CMOS platform. Record level NMOS and PMOS drive currents are achieved for high speed while maintaining low off current of less than 1nA and 1.1 V_{dd} as required for the fast growing mobile low power applications. Compared to SiON-Poly, 30% RO delay reduction has been demonstrated with HK-MG devices.

9.3 - 11:15 a.m.
Variability Aware Modeling and Characterization in Standard Cell in 45nm CMOS with Stress Enhancement Technique, H. Aikawa, E. Morifuji, T. Sanuki, T. Sawada, S. Kyoh, A. Sakata, M. Ohta, H. Yoshimura, T. Nakayama, M. Iwai, F. Matsuoka, Toshiba Corp. Semicoductor Company, Japan

The increasingly significant issue of variability with continued geometry scaling is addressed. Variability caused by layout effects such as stress and rounding effects with lithography have become the critical obstacle against shrinking the design rule and corner margins. Layout dependences for stress enhanced MOSFET including contact positioning, 2^{nd} neighboring poly effect, and bent diffusion are accurately modeled for the first time. With this enhanced variability aware modeling - gate density is increased by selectively pushing the critical design rules to the limit of operation without increasing the circuit margin in 45 nm technology for the first time.

9.4 - 11:40 a.m.
A Scaled Floating Body Cell (FBC) Memory with High-k+Metal Gate on Thin-Silicon and Thin-BOX for 16-nm Technology Node and Beyond, I. Ban, U. Avci, D. Kencke, P. Chang, Intel Corporation, USA

Intel demonstrates a FBC (Floating Body Cell) for the first time utilizing high K / Metal Gate, along with thin (25nm) silicon and thin (10 nm) BOX, separate back gate doping and raised S/D technology enabling memory cell sizes much smaller than 6T-SRAM with feasibility down to 16-nm technology node and beyond. Retention time of 100 mS in devices with 60 nm gate L represents the best retention time for sum 100 nm FBC's. FBC promises much higher density memory for embedded applications compared to conventional embedded SRAM.