2008 VLSI Circuits Short Course

This year the Circuits Short Course is comprised of two programs, Memory and Analog/Digital. The cost of the short course includes both programs and attendees will receive one book for both programs. Attendees will be able to move back and forth between the two programs.

Memory Short Course Program
Embedded Memory Design

Honolulu I
Tuesday, June 17, 8:10 a.m.

Organizers/Chairs: John Barth, IBM
Masao Ito, Renesas Technology Corporation

8:10 a.m. **Introduction**
J. Barth, IBM

8:15 a.m. **Embedded Memory Overview (and DRAM)**
S. Natarajan, TSMC Design Technology Canada

9:25 a.m. **Static RAM**
M. Yamaoka, Hitachi, Ltd.

10:35 a.m. **Break**

10:50 a.m. **Floating Body RAM**
T. Ohsawa, Toshiba Corporation

12:00 p.m. **Lunch**

1:30 p.m. **Phase Change RAM**
C. Lamb, IBM

2:40 p.m. **Break**

2:55 p.m. **Flash**
R. Kakoschke, Infineon

4:05 p.m. **Built in Self Test**
D. Weiss, AMD

5:15 p.m. **Conclusion**
M. Ito, Renesas Technology Corporation

Analog/Digital Short Course Program
Embedded Power Management Circuits and Systems

Honolulu II
Tuesday, June 17, 8:10 a.m.

Organizers/Chairs: Tom Kwan, Broadcom Corporation
Koichi Nose, NEC Corporation

8:10 a.m. **Introduction**
T. Kwan, Broadcom Corporation

8:15 a.m. **Overview of Embedded Power Management Circuits and Systems in SoC's**
D. Anderson, National Semiconductor Corp.

9:25 a.m. **Integrated Power Management for Mobile SoC's**
D. Ho, Broadcom Corporation

10:35 a.m. **Break**

10:50 a.m. **Circuit Design for Power Management Building Blocks**
W.-H. Ki, Hong Kong University of Science and Technology

12:00 p.m. **Lunch**

1:30 p.m. **Thermal Management of High-Performance Processors**
E. Miranda, Analog Devices Corp.

2:40 p.m. **Break**

2:55 p.m. **Power Management at the System/Architecture/Circuit Level**
M. Nomura, NEC

4:05 p.m. **Dynamic Power/Thermal Management in High Performance Processors; Examples and Opportunities**
S. Naffziger, AMD

5:15 p.m. **Speaker Interview Session**

Welcome to the 2008 Symposium on VLSI Circuits

You are cordially invited to attend the 2008 Symposium on VLSI Circuits, to be held on June 18-20th, 2008, at the Hilton Hawaiian Village in Honolulu, Hawaii. Following the rich tradition, the Circuits Symposium will follow the Symposium on VLSI Technology at the same location.

New for this year, the Circuits Symposium will overlap the Technology Symposium by two full days. The two overlap days between Technology and Circuits will allow attendees to freely choose to attend papers from either Symposium, providing a unique opportunity to learn about the latest advances in both VLSI Circuits and Technology, and to interact and exchange ideas with attendees from both Symposia.

Preceding the Symposium on June 17th, two all-day Short Courses on VLSI circuits will be held. For one registration fee, participants can attend either parallel course. The first course, focusing on new challenges facing memory and digital designers is titled "Embedded Memory Design". The other course focuses on the growing challenges in system integration for analog and digital designers and is titled "Embedded Power Management Circuits and Systems."

This year, the technical program committee reviewed 410 papers, selecting 84 outstanding papers for presentation. These papers disclose new developments in Memory, Analog Circuits, Data Converters, Digital Circuits and Processors, and Wireless and Wireline Communication, and represent the leading edge of VLSI circuit design. These papers are in addition to 80 papers from the Technology Symposium. Contributions come from both industry and academia, from around the world.

We have invited two distinguished speakers to describe recent advances and new challenges related to VLSI circuits, technology and applications: "*Next Generation Micro-Power Systems*" by Anantha Chandrakasan of Massachusetts Inst. of Technology and "*Power-Efficient Heterogeneous Parallelism for Digital Convergence*" by Kunio Uchiyama of Hitachi, Ltd.

To complement the formal talks, we have arranged three evening rump sessions on interesting and provocative subjects to give you an opportunity to participate in the discussions and mix with the participants who were chosen to represent contrasting opinions on the topics. The rump sessions explore: "The Future of Silicon Storage – Can Solid State Technologies Take Center Stage?"; "Photons vs. Electrons – Which will Win and When?"; "Ten Years After – Has SOI Finally Arrived?".

Also, new for this year is the Circuits Luncheon on Friday. With a separate fee, you can enjoy an exciting and thought-provoking talk by Tom Lee of Stanford University on "The Great Transatlantic Cable and the Birth of Electrical Engineering." It has limited space and, as with all of Tom Lee's talks, will be very popular. So please do not wait to sign-up!

The rich technical content of the program will undoubtedly interest you, and we certainly hope that it will be a fruitful and enjoyable experience.

This booklet contains the advance program together with the on-line information and forms for the Symposium registration and hotel reservations. Please try to complete these on-line or return these forms as soon as possible. Although the on-site registration will be available at the conference, pre-registration will facilitate Symposium planning.

We look forward to meeting with you at the Symposium in Honolulu.

Katsu Nakamura	Masayuki Mizuno
Program Chair	Program Co-Chair

SESSION 1 – TAPA II
Plenary Session

Wednesday, June 18, 8:25 a.m.
Chairpersons: K. Nakamura, Analog Devices Inc.
M. Mizuno, NEC Corporation

8:25 a.m. **Welcome and Opening Remarks**
S. Kosonocky, AMD
K. Yano, Hitachi Ltd.

1.1 – 8:40 a.m.
Next Generation Micro-Power Systems
A.P. Chandrakasan, D.C. Daly, J. Kwong, Y.K. Ramadass, Massachusetts Institute of Technology

1.2 – 9:25 a.m.
Power-Efficient Heterogeneous Parallelism for Digital Convergence
K. Uchiyama, Hitachi, Ltd.

10:10 a.m. **Break**

SESSION 2 –TAPA I
High-Speed Data Converters

Wednesday, June 18, 10:25 a.m.
Chairpersons: B. Nauta, University of Twente
M. Nagata, Kobe University

2.1 – 10:25 a.m.
A Low Power 6-bit Flash ADC with Reference Voltage and Common-Mode Calibration, C.-Y. Chen, M. Le, K.Y. Kim, Broadcom Corporation, USA

2.2 – 10:50 a.m.
A 7.6 mW 1.75 GS/s 5 Bit Flash A/D Converter In 90nm Digital CMOS, B. Verbruggen, P. Wambacq, M. Kuijk*, G. Van der Plas, IMEC, *Vrije Universiteit, Belgium

2.3 – 11:15 a.m.
A 6-bit 5-GSample/s Nyquist A/D Converter in 65nm CMOS, M. Choi, J. Lee, J. Lee, H. Son, Samsung Advanced Institute of Technology, Korea

2.4 – 11:40 a.m.
A 10.3GS/s 6bit (5.1 ENOB at Nyquist) Time-Interleaved/Pipelined ADC Using Open-Loop Amplifiers and Digital Calibration in 90nm CMOS, A. Nazemi, C. Grace, L. Lewyn, B. Kobeissy, O. Agazzi, P. Voois, C. Abidin, G. Eaton, M. Kargar, C. Marquez, S. Ramprasad, F. Bollo*, V. Posse, S. Wang, G. Asmanis, ClariPhy Communications Inc., USA, *ClariPhy, Argentina

12:05 p.m. **Lunch**

SPECIAL SESSION – TAPA II
Technology Highlights

Wednesday, June 18, 10:25 a.m.
Chairpersons: C. Dennison, Ovonyx Technologies
M. Niwa, Matsushita Electric Ind. Co.

9.1 - 10:25 a.m.
Fully Integrated and Functioned 44nm DRAM Technology for 1GB DRAM, H. Lee, D.-Y. Kim, B.-H. Choi, G.-S. Cho, S.-W. Chung, W.-S. Kim, M.-S. Chang, Y.-S. Kim, J. Kim, H.-J. Lee, H.-S. Song, S.-K. Park, J.-W. Kim, S.-J. Hong, S.-W. Park, Hynix Semiconductor, Korea

9.2 - 10:50 a.m.
A Cost Effective 32nm High-K/ Metal Gate CMOS Technology for Low Power Applications with Single-Metal/Gate-First Process, X. Chen, S. Samavedam*, V. Narayanan, K. Stein, C. Hobbs*, C. Baiocco, W. Li, D. Jaeger, M. Zaleski*, S. Yang, N. Kim**, Y. Lee, D. Zhang*, L. Kang*, J. Chen**, H. Zhuang^, A. Sheikh, J. Wallner, M. Aquilino, J. Han^, Z. Jin, J. Li, G. Massey, S. Kalpat, R. Jha, N. Moumen, R. Mo, S. Kershnan, Z. Wang, M. Chudzik, M. Chowdhury*, D. Nair, C. Reddy*, Y.W. Teh**, C. Kothandaraman, D. Coolbaugh, S. Pandey**, D. Tekleab**, A. Thean*, M. Sherony, C. Lage*, J. Sudijono**, R. Lindsay^, J.-H. Ku^^, M. Khare, A. Steegen, IBM SDRC, *Freescale Semiconductor, **Chartered Semiconductor Manufacturing, ^Infineon Technologies, ^^Samsung Electronics Co., USA

9.3 - 11:15 a.m.
Variability Aware Modeling and Characterization in Standard Cell in 45nm CMOS with Stress Enhancement Technique, H. Aikawa, E. Morifuji, T. Sanuki, T. Sawada, S. Kyoh, A. Sakata, M. Ohta, H. Yoshimura, T. Nakayama, M. Iwai, F. Matsuoka, Toshiba Corp. Semicoductor Company, Japan

9.4 - 11:40 a.m.
A Scaled Floating Body Cell (FBC) Memory with High-k+Metal Gate on Thin-Silicon and Thin-BOX for 16-nm Technology Node and Beyond, I. Ban, U. Avci, D. Kencke, P. Chang, Intel Corporation, USA

12:05 p.m. Lunch

SESSION 3 – TAPA II
Parallel Processing

Wednesday, June 18, 1:30 p.m.
Chairpersons: J. Farrell, AMD
K. Kobayashi, Kyoto University

3.1 – 1:30 p.m.
A 167-processor 65 nm Computational Platform with Per-Processor Dynamic Supply Voltage and Dynamic Clock Frequency Scaling, D. Truong, W. Cheng, T. Mohsenin, Z. Yu, T. Jacobson, G. Landge, M. Meeuwsen, C. Watnik, P. Mejia, A. Tran, J. Webb, E. Work, Z. Xiao, B. Baas, University of California, Davis, USA

3.2 – 1:55 p.m.
A 26mW 6.4GFLOPS Multi-Core Stream Processor for Mobile Multimedia Applications, Y.-M. Tsao, C.-H. Sun, Y.-C. Lin, K.-H. Lok, C.-J. Hsu*, S.-Y. Chien, L.-G. Chen, National Taiwan University, Taiwan, *UMC, Taiwan

3.3 – 2:20 p.m
The Brain Mimicking Visual Attention Engine: An 80x60 Digital Cellular Neural Network for Rapid Global Feature Extraction, S. Lee, K. Kim, M. Kim, J.-Y. Kim, H.-J. Yoo, KAIST, Korea

3.4 – 2:45 p.m.
A 100 GOPS In-vehicle Vision Processor for Pre-crash Safety Systems Based on a Ring Connected 128 4-Way VLIW Processing Elements, S. Kyo, S. Okazaki, T. Koga*, F. Hidano*, NEC Corporation, Japan, *NEC Electronics Corporation, Japan

3:10 p.m. Break

SESSION 4 – TAPA III
Low-Power and Reconfigurable RF

Wednesday, June 18, 1:30 p.m.
Chairpersons: A. Abidi, University of California, Los Angeles
H. Ishikuro, Keio University

4.1 – 1:30 p.m.
A 350uW CMOS MSK Transmitter and 400uW OOK Super-Regenerative Receiver for Medical Implant Communications, J.L. Bohorquez, J.L. Dawson, A.P. Chandrakasan, Massachusetts Inst. of Tech, USA

4.2 – 1:55 p.m.
A 5GHz Fully Integrated Super-regenerative Receiver with On-chip Slot Antenna in 0.13µm CMOS, D. Shi, N. Behdad*, J.-Y. Chen**, M. Flynn, University of Michigan, *University of Central Florida, **ZeroG Wireless Inc., USA

4.3 – 2:20 p.m.
A Direct Conversion Receiver Adopting Balanced Three-phase Analog System, T. Yamaji, T. Itakura, T. Ueno, Toshiba Corporation, Japan

4.4 – 2:45 p.m.
A Direct-Conversion CMOS RF Receiver Reconfigurable from 2GHz to 6GHz, J. Park, S.-N. Kim, J.-H. Seok, Y.-S. Roh, C. Yoo, K. Lim*, J. Kim*, Hanyang University, Korea, *Future Communications IC Inc., Korea

3:10 p.m. Break

SESSION 5 – TAPA II
SRAM Variability

Wednesday, June 18, 3:25 p.m.
Chairpersons: A. Bhavnagarwala, IBM TJ Watson Research Ctr.
T. Sekiguchi, Hitachi, Ltd.

5.1 – 3:25 p.m.
Large-Scale Read/Write Margin Measurement in 45nm CMOS SRAM Arrays, Z. Guo, A. Carlson, L.-T. Pang, K. Duong, T.-J. King Liu, B. Nikolic, University of California, Berkeley, USA

5.2 – 3:50 p.m.
Characterization of Bit Transistors in a Functional SRAM, X. Deng, W.K. Loh, B. Pious, T.W. Houston, L. Liu, B. Khan, D. Corum, J. Raval, J. Gertas, F.-Y. Rousey, J. Steck, C. Suwannakinthorn, R. McKee, Texas Instruments, USA

5.3 – 4:15 p.m
A 0.7V Single-Supply SRAM With 0.495um^2 Cell In 65nm Technology Utilizing Self-Write-Back Sense Amplifier And Cascaded Bit Line Scheme, K. Kushida, A. Suzuki, G. Fukano, A. Kawasumi, O. Hirabayashi, Y. Takeyama, T. Sasaki, A. Katayama, Y. Fujimura,. T. Yabe, Toshiba Corporation, Japan

5.4 – 4:40 p.m.
PVT-Variations and Supply-Noise Tolerant 45nm Dense Cache Arrays with Diffusion-Notch-Free (DNF) 6T SRAM Cells and Dynamic Multi-Vcc Circuits, M. Khellah, N.S. Kim, Y. Ye, D. Somasekhar, T. Karnik, N. Borkar, F. Hamzaoglu, T. Coan, Y. Wang, K. Zhang, C. Webb, V. De, Intel, USA

SESSION 6 – TAPA III
Wireline Signal Conditioning

Wednesday, June 18, 3:25 p.m.
Chairpersons: J. Wieser, National Semiconductor
H. Yamada, Oki Electric Industry Co., Ltd.

6.1 – 3:25 p.m.
A 70dB MTPR Integrated Programmable Gain/Bandwidth 4th-Order Chebyshev Highpass Filter for ADSL/VDSL Receivers in 65nm CMOS, F. Lin, X. Yu, S. Ranganathan, T. Kwan, Broadcom Corporation, USA

6.2 – 3:50 p.m.
A 40Gb/s Low-Power Analog Equalizer in 0.13µm CMOS Technology, J.-H. Lu, K.-H. Chen, S.-I. Liu, National Taiwan Univ., Taiwan

6.3 – 4:15 p.m.
A Merged CMOS Digital Near-End Crosstalk Canceller and Analog Equalizer for Multi-Lane Serial-Link Receivers, J.-H. Lu, K.-H. Chen, A.-M. Lee*, T.-Y. Wu*, S.-I. Liu, National Taiwan University, *Realtek Semiconductor Corp., Taiwan

6.4 – 4:40 p.m.
A 12-Gb/s 11-mW Half-Rate Sampled 5-Tap Decision Feedback Equalizer with Current-Integrating Summers in 45-nm SOI CMOS Technology, T. Dickson, J. Bulzacchelli, D. Friedman, IBM T.J. Watson Res. Ctr, USA

SESSION 7 – TAPA II
Clocking and Signaling

Thursday, June 19, 8:30 a.m.
Chairpersons: K. Shepard, Columbia University
K. Nose, NEC Corporation

7.1 – 8:30 a.m.
Next Generation Intel® Micro-architecture (Nehalem) Clocking Architecture, N. Kurd, J. Douglas, P. Mosalikanti, R. Kumar, Intel Corporation, USA

7.2 – 8:55 a.m.
A Small-Delay Defect Detection Technique For Dependable LSIs, K. Noguchi, K. Nose, T. Ono*, M. Mizuno, NEC Corporation, *NEC Electronics Corporation, Japan

7.3 – 9:20 a.m.
Sensor Data Retrieval Using Alignment Independent Capacitive Signaling, Y.-S. Lin, D. Sylvester, D. Blaauw, University of Michigan, USA

7.4 – 9:45 a.m.
Characterizng Sampling Aperture of Clocked Comparators, M. Jeeradit, J. Kim, B. Leibowitz, P. Nikaeen*, V. Wang**, B. Garlepp^, C. Werner, Rambus Inc., *Stanford University, **University of California, Los Angeles, ^SiTime Corp, USA

10:10 a.m. Break

SESSION 8 – TAPA III
Data Converters and Biomedical Circuits

Thursday, June 19, 8:30 a.m.
Chairpersons: L. Breems, NXP Semiconductors
M. Ito, Renesas Technology Corporation

8.1 – 8:30 a.m.
A 1.2V 30mW 8b 800MS/s Time-Interleaved ADC in 65nm CMOS, W.-H. Tu, T.-H. Kang, MediaTek Inc. Taiwan

8.2 – 8:55 a.m.
A 1.2V 250mW 14b 100MS/s Digitally Calibrated Pipeline ADC in 90nm CMOS, H. Van de Vel, B. Buter, H. van der Ploeg, M. Vertregt, G. Geelen, E. Paulus, NXP Semiconductors, The Netherlands

8.3 – 9:20 a.m.
A 64 Channel Programmable Closed-loop Deep Brain Stimulator with 8 Channel Neural Amplifier and Logarithmic ADC, J. Lee, H.-G. Rhew, D. Kipke, M. Flynn, University of Michigan, USA

8.4 – 9:45 a.m.
A 1-V 450-nW Fully Integrated Biomedical Sensor Interface System, X. Xu, X. Zou, L. Yao, Y. Lian, National University of Singapore, Singapore

10:10 a.m. Break

SESSION 9 – TAPA II
Frequency Synthesis Components

Thursday, June 19, 10:25 a.m.
Chairpersons: A. Amerasekera, Texas Instruments
J. Lee, National Taiwan University

9.1 – 10:25 a.m.
An Efficient High-Resolution 11-Bit Noise-Shaping Multipath Gated Ring Oscillator TDC, M. Straayer, M. Perrott, Massachusetts Institute of Technology, USA

9.2 – 10:50 a.m.
Digital Frequency Detector based on Multiphase Ring Oscillator, C.-Y. Cha, M. Lee*, J. Lee, T. Kim, Samsung Advanced Institute of Technology, Korea, *University of California, Los Angeles, USA

9.3 – 11:15 a.m.
93.5~109.4GHz CMOS Injection-Locked Frequency Divider With 15.3% Locking Range, L.-C. Cho, K.-H. Tsai, C.-C. Hung, S.-I. Liu, National Taiwan University, Taiwan

9.4 – 11:40 a.m.
A 2.5-GHz 860μW Charge-Recycling Fractional-N Frequency Synthesizer in 130nm CMOS, D. Park, W. Lee, S. Jeon, S.H. Cho, KAIST, Korea

12:05 p.m. Lunch

SESSION 10 – TAPA III
Multi-Standard RF

Thursday, June 19, 10:25 a.m.
Chairpersons: J. Dawson, Massachusetts Institute of Technology
S. Mutoh, NTT Corporation

10.1 – 10:25 a.m.
A Wideband Supply Modulator for 20MHz RF Bandwidth Polar PAs in 65nm CMOS, R. Shrestha, R. van der Zee, A. de Graauw*, B. Nauta, University of Twente, *NXP, The Netherlands

10.2 – 10:50 a.m.
A Multi-Mode Multi-band CMOS Direct-Conversion Mobile-TV Tuner for DVB-H/T and T-DMB/DAB Applications, M.-W. Hwang, M. Ahn, S. Beck, J.-C. Lee, S. Hong, S. Lee, S. Jeong, S. Lim, H. Cho, Y.-J. Kim*, I.-C. Hwang**, J. Kim, Future Communications IC Inc., *Korea Acrospace University, **Kangwon National University, Korea

10.3 – 11:15 a.m.
A Quad Band WCDMA Transceiver with Fractional Local Divider, H. Kamizuma, T. Yamawaki, Y. Akamine, K. Maeda, S. Tanaka, K. Hikasa*, Hitachi Central Research Laboratory, *Renesas Technology

10.4 – 11:40 a.m.
All-Digital Out-phasing Modulator for a Software-Defined Transmitter, M. Heidari, M. Lee, A. Abidi, University of California, Los Angeles, USA

12:05 p.m. Lunch

SESSION 11 – TAPA II
Processors for HDTV

Thursday, June 19, 1:30 p.m.
Chairpersons: B. Nikolic, University of California, Berkeley
H. Kabuo, Matsushita Electric Ind. Co., Ltd.

11.1 – 1:30 p.m.
A 256mW Full-HD H.264 High-Profile CODEC Featuring Dual Macroblock-Pipeline Architecture in 65nm CMOS, K. Iwata, S. Mochizuki, T. Shibayama, F. Izuhara, H. Ueda, K. Hosogi*, H. Nakata*, M. Ehama*, T. Kengaku, T. Nakazawa, H. Watanabe, Renesas Technology Corp., *Hitachi Ltd., Japan

11.2 – 1:55 p.m.
An H.264/AVC Scalable Extension and High Profile HDTV 1080p Encoder Chip, Y.-H. Chen, T.-D. Chuang, Y.-J. Chen, C.-T. Li, C.-J. Hsu*, S.-Y. Chien, L.-G. Chen, National Taiwan University, *UMC, Taiwan

11.3 – 2:20 p.m.
An H.264/AVC High422 Profile and MPEG-2 422 Profile Encoder LSI for HDTV Broadcasting Infrastructures, K. Nitta, M. Ikeda, H. Iwasaki, T. Onishi, T. Sano, A. Sagata, Y. Nakajima, M. Inamori, T. Yoshitome, H. Matsuda, R. Tanida, A. Shimizu, J. Naganuma, K. Nakamura, Nippon Telegraph and Telephone Corporation, Japan

11.4 – 2:45 p.m.
A 2/4/8 Antennas Configurable Diversity OFDM Receiver For Mobile HDTV Application, T. Wada, T. Iida**, H. Mizutani*, S. Sakaguchi*, S. Murakami*, A. Shimizu**, University of the Ryukyus, *Magna Design Net, Inc., **Sanyo Electric Co., Japan

3:10 p.m. Break

SESSION 12 – TAPA III
PLLs and Wireless Transceivers

Thursday, June 19, 1:30 p.m.
Chairpersons: C.-M. Hung, Texas Instruments
M. Ikeda, University of Tokyo

12.1 – 1:30 p.m.
A Low Noise, Wideband Digital Phase-Locked Loop Based On A New Time-To-Digital Converter With Subpicosecond Resolution, M. Lee, M. Heidari, A. Abidi, University of California, Los Angeles, USA

12.2 – 1:55 p.m.
A 0.4ps-RMS-Jitter 1-3GHz Ring-Oscillator PLL using Phase-Noise Preamplification, Z. Cao, Y. Li*, S. Yan, University of Texas at Austin, *Analog Devices, USA

12.3 – 2:20 p.m.
RF Transceiver and Wireless Calibration of On-Chip Frequency Reference for a True Single Chip Radio, Y. Ding, Y. Su, C. Cao, J.-J. Lin, T. Wu, M. Hwang, R. Fox, J. Brewer, K. O, University of Florida, USA

12.4 – 2:45 p.m.
A 100Mbps, 0.41mW, DC-960MHz Band Impulse UWB Transceiver in 90nm CMOS, L. Liu, Y. Miyamoto, Z. Zhou, K. Sakaida, R. Jisun, K. Ishida, M. Takamiya, T. Sakurai, University of Tokyo, Japan

3:10 p.m. Break

SESSION 13 – TAPA II
Low Power Memory and Interface Techniques

Thursday, June 19, 3:25 p.m.
Chairpersons: O. Jungroth, Intel Corporation
K. Kajigaya, Elpida Memory, Inc.

13.1 – 3:25 p.m.
A Fully Logic-Process-Compatible, 3-Transistor, SESO-memory Cell Featuring 0.1-FIT/Mb Soft Error, 100-MHz Random Cycle, and 100-ms Retention, N. Kameshiro, T. Watanabe, T. Ishii, T. Mine, T. Sano*, H. Ibe, S. Akiyama, K. Yanagisawa**, T. Ipposhi**, T. Iwamatsu**, Y. Takahashi**, Hitachi Ltd., *Renesas Northern Japan Semiconductor Inc., **Renesas Technology Corp., Japan

13.2 – 3:50 p.m.
Novel Co-design of NAND Flash Memory and NAND Flash Controller Circuits for Sub-30nm Low-Power High-Speed Solid-State Drives (SSD), K. Takeuchi, University of Tokyo, Japan

13.3 – 4:15 p.m.
A 16Gb/s/link, 64GB/s Bidirectional Asymmetric Memory Interface Cell, K. Chang, H. Lee, J.-H. Chun, T. Wu, T.J. Chin, K. Kaviani, J. Shen, X. Shi, W. Beyene, Y. Frans, B. Leibowitz, N. Nguyen, F. Quan, J. Zerbe, R. Perego, F. Assaderaghi, Rambus Inc., USA

13.4 – 4:40 p.m.
A 16-Gb/s Differential I/O Cell with 380fs RJ in an Emulated 40nm DRAM Process, N. Nguyen, Y. Frans, B. Leibowitz, S. Li, R. Navid, M. Aleksic, F. Lee, F. Quan, J. Zerbe, R. Perego, F. Assaderaghi, Rambus Inc., USA

SESSION 14 – TAPA III
Power Management Circuits and Image Sensor

Thursday, June 19, 3:25 p.m.
Chairpersons: T. Kwan, Broadcom Corp.
M. Igarashi, Sony Corp.

14.1 – 3:25 p.m.
Single-Inductor Dual-Output DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices, M.-H. Huang, K.-H. Chen, W.-H. Wei*, National Chiao Tung University, *Richtek Technology Corp., Taiwan

14.2 – 3:50 p.m.
Adaptive Step-Down Switched-Capacitor Power Converter with *z*-Domain Observation-Based Line-Load Regulation, M. Song, I. Chowdhury, D. Ma, A.P. Brokaw*, University of Arizona, *Analog Devices, USA

14.3 – 4:15 p.m.
An SC Voltage Regulator with Novel Area-Efficient Continuous Output Regulation by Dual-Branch Interleaving Control Scheme, F. Su, W.-H. Ki, C.-Y. Tsui, Hong Kong University of Science and Technology, Hong Kong

14.4 – 4:40 p.m.
A Very Low Column FPN and Row Temporal Noise 8.9M-Pixel, 60 fps CMOS Image Sensor with 14bit Column Parallel SA-ADC, S. Matsuo, T. Bales, M. Shoda, S. Osawa, B. Almond*, Y. Mo**, J. Gleason**, T. Chow**, I. Takayanagi, Micron Japan Ltd., Japan, *Micron Europe, United Kingdom, **Micron Technology, USA

JOINT TECHNOLOGY/CIRCUITS RUMP SESSION
Tuesday, June 17
8:00 p.m – 10:00 p.m.

Organizers:

Circuits	**Technology**
G. Lehmann, Infineon	T. Grider, Texas Instruments
K. Arimoto, Renesas	Y. Omura, Kansai University

RJ1: Ten years after – Has SOI finally arrived?
Tapa I

Moderators: L. Counts, LC Consulting
K. Ishimaru, Toshiba America

Ten years after introduction of SOI into a production as a competitor to bulk-CMOS, both technologies continue to co-exist in some of the application domains, such as microprocessors and gaming. On the other hand, mainstream SoC's exclusively use bulk-CMOS. A panel similar to this one 10 years ago has concluded that SOI has a performance advantage over bulk, and the cost will be its main barrier for wide adoption. Has anything changed and will it change in the next decade? Will SOI penetrate more market segments or disappear? Does further technology scaling require the migration to fully-depleted SOI?

Panelists:

M. Bohr, Intel	R. Mahnkopf, Infineon
G. Shahidi, IBM	C. Mazure, SOITEC
E. Suzuki, AIST	D. Scott, TSMC
A. Kameyama, Toshiba	M. Usami, Hitachi

CIRCUITS RUMP SESSION
Thursday, June 19
8:00 p.m. – 10:00 p.m.

Organizers: B. Nikolic, University of California, Berkeley
T. Sekiguchi, Hitachi, Ltd.

R1: Photons vs. Electrons – Which Will Win and When? (The Ongoing Race for Short-Distance High-Speed Data Connectivity)
Honolulu I
Organizers: J. Savoj, Qualcomm
M. Fukaishi, NEC

Moderator: J. Wieser, National Semicondcutor

This session discusses the utilization of copper and optical interconnects for high-speed chip-to-chip interfaces, along with the emergence of new disruptive technologies. The panel focuses on high-speed short-range and medium-range data connectivity and issues regarding the design of transceivers for these systems, as well as the roadmap of IOs for future high-performance/low-power/small-form-factor systems.

Panelists:

M. Horowitz, Stanford Universty	I. Young, Intel
J. D'Ambrosia, Force10 Networks	S. Kasturia, Teranetics
H. Tamura, Fujitsu Japan	Y. Ohtomo, NTT Japan

R2: The Future of Silicon Storage – Can Solid State Technologies Take Center Stage?

Honolulu II

Organizers: A. Bhavnagarwala, IBM
S. Ohshima, Toshiba

Moderator: A. Bhavnagarwala, IBM

With the market for storage class memories projected to exceed 500 ExaBytes* by 2012, and NAND Flash and DDR based solid state drives (SSD) already making inroads into the enterprise sector of storage and into niche applications, will the continued scaling of SSD cost enable silicon to take center stage in storage? Or, would Hard Disk Drives, with Heat Assisted Magnetic Recording and Bit Patterned Media - projected to exceed densities of 50 Terabits/in2, continue to dominate as the technology of choice? A panel of experts from across the industry will present their vision of opportunities and limitations of emerging and incumbent storage technologies that can potentially satisfy the mass storage market created by the proliferation of digital content. (*Gartner)

Panelists:

C. Lam, IBM	K. Tsuchiya, Toshiba
K. Quader, SanDisk	K. Kim, Samsung
M. Kryder, Carnegie Mellon	H.-S.P. Wong, Stanford
S. Lai, Ovonyx	

SESSION 15 – TAPA I
Power-Aware Circuit Techniques

Friday, June 20, 8:15 a.m.

Chairpersons: J. Barth, IBM Microelectronics
T. Shiota, Fujitsu Laboratories, Ltd.

15.1 – 8:15 a.m.

A Sub-µs Wake-up Time Power Gating Technique with Bypass Power Line for Rush Current Support, K. Kawasaki, T. Shiota, K. Nakayama, A. Inoue, Fujitsu Laboratories Ltd., Japan

15.2 – 8:40 a.m.

Dynamic Voltage Boost (DVB) Method for Improving Power Integrity of Low-Power Multi-Processor SoCs, Y. Kanno, K. Yoshizumi, Y. Yasu, K. Ishibashi, H. Mizuno, Hitachi Ltd., Japan

15.3 – 9:05 a.m.

Experimental Evaluation of Digital-Circuit Susceptibility to Voltage Variation in Dynamic Frequency Scaling, M. Fukazawa, M. Kurimoto**, R. Akiyama*, H. Takata**, M. Nagata, Kobe University, *Renesas Technology Corp., ** Renesas Design, Japan

15.4 – 9:30 a.m.
A 1.1V 35µm × 35µm Thermal Sensor With Supply Voltage Sensitivity Of 2ºC/10%-Supply For Thermal Management On The SX-9 Supercomputer, E. Saneyoshi, K. Nose, M. Kajita, M. Mizuno, NEC Corporation, Japan

9:55 a.m. **Break**

SESSION 16 – TAPA II
60-120GHz Wireless Receivers

Friday, June 20, 8:15 a.m.
Chairpersons: F. Dai, Auburn University
K. Agawa, Toshiba

16.1 – 8:15 a.m.
A 1Gbps Mixed-Signal Analog Front End for a 60GHz Wireless Receiver, D.A. Sobel, R.W. Brodersen, University of California, Berkeley, USA

16.2 – 8:40 a.m.
19.2mW 2Gbps CMOS Pulse Receiver for 60GHz Wireless Communication, A. Oncu, M. Fujishima, University of Tokyo, Japan

16.3 – 9:05 a.m.
A Dual-band 61.4~63GHz/75.5~77.5GHz CMOS Receiver in a 90nm Technology, K.-H. Chen, C. Lee, S.-I. Liu, National Taiwan University, Taiwan

16.4 – 9:30 a.m.
Circuit Performance Characterization of Digital 45-nm CMOS Technology for Applications around 110GHz, R.A. Aroca, A. Tomkins, Y. Doi*, T. Yamamoto*, S.P. Voinigescu, University of Toronto, Canada, *Fujitsu Laboratories Ltd., Japan

9:55 a.m. **Break**

SESSION 17 – TAPA I
High Speed Timing Circuits

Friday, June 20, 10:10 a.m.
Chairpersons: S. Tam, Intel Corporation
J.-Y. Sim, POSTECH

17.1 – 10:10 a.m.
Time-to-Digital Converter with Vernier Delay Mismatch Compensation for High Resolution On-Die Clock Jitter Measurement, T. Hashimoto, H. Yamazaki, A. Muramatsu, T. Sato, A. Inoue, Fujitsu Laboratories Limited, Japan

17.2 – 10:35 a.m.
In-Situ Jitter Tolerance Measurement Technique for Serial I/O, J. Jaussi, G. Balamurugan, J. Kennedy, F. O'Mahony, M. Mansuri, R. Mooney, B. Casper, U.-K. Moon*, Intel Corporation, *Oregon State University, USA

17.3 – 11:00 a.m.
Phase Correction of a Resonant Clocking System Using Resonant Interpolators, L.-M. Lee, C.-K.K. Yang, University of California, Los Angeles, USA

17.4 – 11:25 a.m.
A Multi Standard 1.5 to 10Gb/s Latch-Based 3-Tap DFE Receiver with a SSC Tolerant CDR for Serial Backplane Communication, M. Pozzoni, S. Erba, P. Viola, M. Pisati, E. Depaoli, D. Sanzogni, R. Brama**, D. Baldi, M. Repossi, F. Svelto*, STMicroelectronics, *Universita degli Studi di Pavia, **Universita di Modena e Reggio Emilia, Italy

11:50 p.m. Lunch

SESSION 18 – TAPA II
Oversampled Data Converters

Friday, June 20, 10:10 a.m.
Chairpersons: J. Gealow, MediaTek Wireless, Inc.
M. Ito, Renesas Technology Corporation

18.1 – 10:10 a.m.
A 1.3-mW per-Channel 103-dB SNR Stereo Audio DAC with Class-D Head-Phones Amplifier in 65nm CMOS, Y.-H. Lee, C.-K. Seok, B.-J. Kim, S.-B. You, W.-S. Yeum, H.-J. Park, Y.-H. Jun, B.-S. Kong*, J.-W. Kim, Samsung Electronics, *Sungkyunkwan University, Korea

18.2 – 10:35 a.m.
A 0.7-V 100-dB 870-µW Digital Audio Σ Δ Modulator, H. Park, K. Nam, D. Su, K. Vleugels, B. Wooley, Stanford University, USA

18.3 – 11:00 a.m.
A 2.1mW/3.2mW Delay-Compensated GSM/WCDMA Σ Δ Analog-Digital Converter, M. Vadipour, C. Chen, A. Yazdi, M. Nariman, T. Li, P. Kilcoyne, H. Darabi, Broadcom Corporation, USA

18.4 – 11:25 a.m.
A 14b 23MS/s 48mW Resetting Σ Δ ADC with 87dB SFDR 11.7b ENOB & 0.5mm^2 Area, C. Lee, M. Flynn, University of Michigan, USA

11:50 p.m. Lunch

HONOLULU SUITE
2008 Circuits Luncheon
(Separate Registration Required)

Friday, June 20, 12:00 p.m.

The Great Transatlantic Cable and the Birth of Electrical Engineering, Tom Lee, Stanford University

The name Cyrus Field should be much more widely known than it is, particularly among electrical engineers. For we have him to thank for the 19th century's equivalent of the Moon program; the laying of the first transatlantic telegraph cable. Spanning the Atlantic without amplifiers isn't as easy as it sounds. Field's multiple attempts between 1858 and 1866 were punctuated by humiliating failure and the American Civil War. A board of inquiry convened in the aftermath of the first failure, identified several problems, including Field's near total reliance on a medical doctor for technical advice, as well as a frustrating lack of a technical vocabulary even to describe aspects of the failure itself. The response to this analysis was the creation of the language and profession of electrical engineering with William Thomson, as new technical lead for the project. He was perhaps the first professional electrical engineer. For making the 1866 cable a success, Thomson was knighted that year and eventually became Lord Kelvin. This talk will describe the technical history of the cable project with a focus on how it established electrical engineering as a profession.

To register for the luncheon, please refer to the registration form for fee information.

SESSION 19 – TAPA I
Power-Aware Processing

Friday, June 20, 1:30 p.m.
Chairpersons: V. De, Intel Corporation
M. Hariyama, Tohoku University

19.1 – 1:30 p.m.
A Powerful Yet Ecological Parallel Processing System Using Execution-Based Adaptive Power-Down Control And Compact Quadruple-Precision Assist FPUs, H. Aoki, T. Kawahara, M. Yamaoka, C.Yoshimura, Y. Nagasaka, K. Takayama, N. Sukegawa, Y. Fukumura, M. Nakahata, H. Sawamoto, M. Odaka, T. Sakurai*, K. Kasai, Hitachi Ltd., *University of Tokyo, Japan

19.2 – 1:55 p.m.
The Phoenix Processor: A 30pW Platform for Sensor Applications, M. Seok, S. Hanson, Y.-S. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, D. Blaauw, University of Michigan, USA

19.3 – 2:20 p.m.
An Asynchronous Power Aware and Adaptive NoC Based Circuit, E. Beigne, F. Clermidy, J. Durupt, H. Lhermet, S. Miermont, Y. Thonnart, T. Tran-Xuan, A. Valentian, D. Varreau, P. Vivet, CEA-LETI MINATEC, France

19.4 – 2:45 p.m.
DSP Architecture Optimization in Matlab/Simulink Environment, R. Nanda, C.-H. Yang, D. Markovic, University of California, Los Angeles, USA

3:10 p.m. Break

SESSION 20 – TAPA II
High Speed Transceivers

Friday, June 20, 1:30 p.m.
Chairpersons: J. Savoj, Qualcomm
J. Lee, National Taiwan University

20.1 – 1:30 p.m.
A 40-Gb/s Transceiver in 0.13-µm CMOS Technology, J.-K. Kim, J. Kim**, G. Kim*, H. Chi, D.-K. Jeong, Seoul National University, Korea, *Silicon Image, **Rambus Inc., USA

20.2 – 1:55 p.m.
A 7.5Gb/s Transmitter with Self-Adaptive FIR, D. Tonietto, J. Hogeboon, E. Bensoudane, S. Sadeghi, H. Khor, P. Krotnev, STMicroelectronics, Canada

20.3 – 2:20 p.m.
A TeraBit/s-Throughput, SerDes-Based Interface for a Third-Generation 16 Core 32 Thread Chip-Multithreading SPARC Processor, J. Nasrullah, A. Amin, W. Ahmad, Z. Qin, Z. Mushtaq, O. Javed, J. Yoon, L. Chua, D. Huang, B. Huang, M. Vichare, K. Ho, M. Rashid, Sun Microsystems, USA

20.4 – 2:45 p.m.
A 21-Channel 8Gb/s Transceiver Macro with 3.6ns Latency in 90nm CMOS for 80cm Backplane Communication, A. Hayashi, M. Kuwata, K. Suzuki, T. Muto, M. Tsuge, K. Nagashima, D. Hamano, T. Usugi, K. Nakajima, M. Ogihara, N. Mikami*, K. Watanabe, Hitachi Ltd., *Hitachi ULSI Systems, Japan

3:10 p.m. Break

SESSION 21 – TAPA I
Cache and Embedded Memories

Friday, June 20, 3:25 p.m.
Chairpersons: G. Lehmann, Infineon Technologies
C. Kim, Samsung Electronics Co., Ltd.

21.1 – 3:25 p.m.
A One MB Cache Subsystem Prototype with 2GHz Embedded DRAMs in 45nm SOI CMOS, P. Klim, J. Barth, W. Reohr*, D. Dick, G. Fredeman, G. Koch, H. Le, A. Khargonekar, P. Wilcox, J. Golz, J.B. Kuang*, A. Mathews, T. Luong, H. Ngo, R. Freese**, H. Hunter*, E. Nelson, P. Parries, T. Kirihata, S. Iyer, IBM Systems and Technology Group, *IBM Research Division, **Advanced Micro Devices, USA

21.2 – 3:50 p.m.
A High Performance 2.4 Mb L1 and L2 Cache Compatible 45nm SRAM with Yield Improvement Capabilities, R. Joshi, R. Houle, D. Rodko, P. Patel, W. Huott, R. Franch, Y. Chan, D. Plass, S. Wilson, S. Wu, R. Kanj, IBM, USA

21.3 – 4:15 p.m.
A 0.6V 45nm Adaptive Dual-rail SRAM Compiler Circuit Design for Lower VDD_min VLSIs, Y.H. Chen, W.M. Chan, S.Y. Chou, H.J. Liao, H.Y. Pan, J.J. Wu, C.H. Lee, S.M. Yang, Y.C. Liu, H. Yamauchi*, TSMC, Taiwan, *Fukuoka Institute of Technology, Japan

21.4 – 4:40 p.m.
A 45-nm Single-port and Dual-port SRAM Family with Robust Read/Write Stabilizing Circuitry under DVFS Environment, K. Nii, M. Yabuuchi, Y. Tsukamoto, S. Ohbayashi, Y. Oda*, K. Usui**, T. Kawamura, N. Tsuboi, T. Iwasaki, K. Hashimoto, H. Makino, H. Shinohara, Renesas Technology Corporation, *Shikino High-Tech Corporation, **Daioh Electric Corporation, Japan

SESSION 22 – TAPA II
Pipelined A/D Converters

Friday, June 20, 3:25 p.m.
Chairpersons: K. Gulati, Cambridge Analog Technologies Inc.
M. Nagata, Kobe University

22.1 – 3:25 p.m.
A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Residue Amplification, J. Hu, N. Dolev, B. Murmann, Stanford University, USA

22.2 – 3:50 p.m.
A Fully-Differential Zero-Crossing-Based 1.2V 10b 26MS/s Pipelined ADC in 65nm CMOS, S.-K. Shin, Y.-S. You, S.-H. Lee, K.-H. Moon, J.-W. Kim, L. Brooks*, H.-S. Lee*[1,*2], Samsung Electronics, Korea, *[1]Massachusetts Institute of Technology, USA, *[2]Cambridge Analog Technologies, Inc., USA

22.3 – 4:15 p.m.
A 12b 50MS/s 10.2mA 0.18µm CMOS Nyquist ADC with a Fully Differential Class-AB Switched OP-AMP, H.-C. Choi, Y.-J. Kim, M.-H. Lee, Y.-L. Kim, S.-H. Lee, Sogang University, Korea

22.4 – 4:40 p.m.
A Process-Scalable Low-Power Charge-Domain 13-bit Pipeline ADC, M. Anthony, E. Kohler, J. Kurtze, L. Kushner, G. Sollner, Kenet Inc., USA

GENERAL INFORMATION

SCOPE OF SYMPOSIUM

The scope of the Symposium covers all aspects of VLSI circuits, such as circuit design to address challenges of deeply scaled technologies; digital circuit and mixed signal circuits such as data converters and amplifiers to address performance; power, technology scaling, and variability; complex SOC systems describing new architectures and implementations; circuit approaches for clock generation and distribution; advances in memory circuits; especially for embedded memories in scaled technologies; adaptive power techniques and power management for analog and digital circuits; techniques for digitally-assisted analog and analog-assisted digital including digital implementation of previously analog functions; architectures and circuits for RF and wireless communications; circuits for sensors and displays; wireline transceiver and I/O design optimized for high bandwidth and low-power spanning from chip-to-chip through long-reach applications; fundamentals related to the above, including innovative transistor-level circuit design and circuits for characterizing technology changes and variations.

REGISTRATION INFORMATION

The VLSI Symposia encourages all participants to register on-line. To register on-line, go to www.vlsisymposium.org. All payments must be paid in US dollars by credit card or check. No bank transfers are allowed. The deadline to register is May 27, 2008. **After May 27, 2008 you must register on-site. If you register on-site, an additional $75 will be added to the registration fees.**

Payment of the registration fee entitles the registrant to one copy of the Technical Digest, one CD-ROM, all coffee breaks, one banquet and one reception ticket.

	Member	NonMember	Students
Tech Short Course	$270	$295	$75
Tech Symposium	$525	$600	$250
Circ Short Course	*$325*	*$350*	*$100*
Circ Symposium	$525	$600	$250
Circuits Luncheon	$50	$50	$50
Digest	$75	$75	$75
Add'l Short Course books	$95	$95	$95
Banquet Tickets	$75	$75	$75

*(**This year the Circuits Short Course is comprised of two programs, Analog/Digital and Memory. The cost of the short course includes both programs and attendees will receive one book for both programs. Attendees will be able to move back and forth between the two programs.)*

REGISTRATION: Credit Cards (MasterCard/Visa/Amex), personal checks, company checks or traveler's checks payable to the 2008 VLSI Symposia **in U.S. Dollars** are the only acceptable forms of payment. All checks must be drawn on U.S. banks. Registration not conforming to these guidelines will be returned. Please

complete the Registration Card (see centerfold) and return with payment of the appropriate registration fees **no later than May 27, 2008** to VLSI c/o Yes Events, PO Box 32862, Baltimore, MD 21282, USA Telephone: US Reg: 1-800-937-8728, Int'l Reg: +1-410-559-2236 Fax: +1-410-559-2217
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There will be a fee of $30 for all cancellations. No refunds will be issued for cancellations received after May 27, 2008. All refunds will be processed after the Symposia.

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A block of rooms has been reserved at the Hilton Hawaiian Village for 2008 VLSI Symposia participants. RESERVATIONS MUST BE RECEIVED BY May 19, 2008 to qualify for our special room rates:

	Single/Double
Garden View	$215.00
Partial Ocean View	$259.00
Ocean View	$279.00
Deluxe Ocean View	$299.00
Alii Ocean View	$325.00

All rooms are subject to an 11.96% combined tax. To make a room reservation, go to www.vlsisymposium.org, click the tab at the top of the screen labeled Travel/Reservation Information. Click on the link for the hotel reservations.

OR, complete the Hotel Reservation Form and return it directly to the Hilton Hawaiian Village no later than May 19, 2008. All reservations must be accompanied by advanced deposit or guaranteed by a credit card in order to guarantee the reservation. A confirmation will be mailed to you directly by the hotel. Check-in time is 2:00 pm and check-out is 11:00 am.

The hotel offers both non-smoking and handicapped rooms. Please make these specific requests when you make your hotel reservation.

TRANSPORTATION FROM THE HONOLULU INTERNATIONAL AIRPORT TO THE HILTON HAWAIIAN VILLAGE: Airport Express Shuttle and taxi services are available from the Honolulu International Airport to the hotel and return. Shuttle fare is approximately $12.00 each way. From the hotel to the airport you need to make a reservation one day in advance. Taxi fare is approximately $30.00 one way.

VISA REQUIREMENTS FOR ENTRY INTO U.S.: Citizens of foreign countries must have in their possession a valid passport and visa upon entering the United States. Foreign participants should contact the United States Embassy, Consulate, or Office of Tourism in their home country AS SOON AS POSSIBLE to determine their particular visa requirements.

SYMPOSIA REGISTRATION DESK: The Symposia Registration Desk, located in the Palace Lounge Lobby will be open as follows:

Symposia Registration

Sunday, June 15	4:00 pm – 6:00 pm
Monday, June 16	7:30 am - 5:00 pm
Tuesday, June 17	7:30 am - 5:00 pm
Wednesday, June 18	7:30 am - 5:00 pm
Thursday, June 19	8:00 am – 5:00 pm
Friday, June 20	8:00 am – 3:00 pm

VLSI CIRCUITS SYMPOSIUM RECEPTION: A reception will be held on Tuesday, June 17 from 6:00 pm to 8:00 pm on the Lagoon Green.

SYMPOSIA ON VLSI TECHNOLOGY AND VLSI CIRCUITS BANQUET: The 2008 Symposia on VLSI Technology and VLSI Circuits Banquet will be held on Wednesday, June 18 on the Lagoon Green from 7:00 pm to 9:00 pm. Banquet tickets for accompanying guests can be purchased at the Registration desk in the Palace Lounge Lobby.

SPEAKER PREPARATION CENTER: There will be a designated Speaker Preparation Room. Specifics will be available at the Registration Desk located in the Palace Lounge Lobby.

DIGEST: Registrants will receive (1) copy of the Digest and (1) copy of the CD-Rom when they pick up their Symposium materials at the Registration Desk. Additional copies of the Digest will be available on-site for $75. Following the Symposium, additional copies of the Digest will be available through IEEE Single Copy Sales, 445 Hoes Lane, Piscataway, NJ 08855, USA +1 732-981-0060 or (Toll free) 1 800-678-4333.

TRAVEL EXPENSE SUPPORT: Requests for partial travel expense support for students who are presenting papers should be sent to: the Secretariat USA, 19803 Laurel Valley Place, Montgomery Village, MD, 20886 USA Fax: 301-527-0994 Email: vlsi@vlsisymposium.org **no later than April 25, 2008**. All travel support will be paid after the Symposia.

MESSAGE CENTER: The Message Board will be located in the Palace Lounge Lobby adjacent to the Registration Desk. Please advise those who wish to reach you during the day to contact the Hilton Hawaiian Village at 808-949-4321 and request the VLSI Symposia Message Desk. Facsimiles clearly marked with both the recipient's name and the name of the Symposia may be sent to 808-947-7914.

ADDITIONAL INFORMATION: Additional information is available at: http://www.vlsisymposium.org

To obtain an Advance Program and other general information or to be placed on the Symposia mailing list, please contact:

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