2008 VLSI Technology Short Course
TAPA I/II

CMOS Logic – Technology Challenges for the Transition from 32nm to 22nm

Monday, June 16, 8:10 a.m.

Organizers: Klaus Schruefer, Infineon Technologies
Satoshi Inaba, Toshiba Corporation
Digh Hisamoto, Hitachi Ltd.

8:10 a.m.	**Introduction** K. Schruefer, Infineon Technologies
8:15 a.m.	**Lithography Solutions** M. Colburn, IBM Corporation
9:25 a.m.	**FEOL Scaling, New Device Architectures and Materials** J. Kavalieros, Intel Corporation
10:35 a.m.	**Break**
10:50	**Interconnect Scaling, Processes and Integration** H.-J. Barth, Infineon Technologies
12:00 p.m.	**Lunch**
1:30 p.m.	**System on Chip – Key Aspects for MS/RF Integration** M. Huang, Freescale
2:40 p.m.	**Break**
2:55 p.m.	**Embedded Memory: SRAM** Y. Kim, Samsung Electronics
4:05 p.m.	**Variability and DFM** H. Yoshimura, Toshiba Corporation
5:15 p.m.	**Conclusion**

Welcome to the 2008 Symposium on VLSI Technology!

On behalf of the organizing Committees, it is our pleasure to invite you to attend the 2008 Symposium on VLSI Technology which will be held from June 17-19 in Honolulu, Hawaii.

Since its founding in 1982, this symposium has been one of the most prestigious international forums for the latest research and development in VLSI technology. The program committee has worked very hard this year to select 80 excellent contributed and invited papers and organized them into 21 sessions. We are delighted to have two distinguished Invited Speakers for the Plenary Session.

Dr. Mark Pinto of Applied Materials will present a talk titled: "*Has the Sun Finally Risen on Photovoltaics*?" and Dr. Makoto Ishida of Toyohashi University of Technology will speak on "*Silicon Smart Microchips for Intelligent Sensing*"

The conference will also have three Rump Sessions on the evening of June 17 as a means to facilitate informal discussions among researchers. One is a joint session with the Symposium on VLSI Circuits which will ask the question: "Ten years after – Has SOI finally arrived?"

The other two sessions will cover specific technology related topics of current interest;
- Who will keep SRAM scaling alive by 2012: Designers or Technologists
- More than Moore – Functional Diversification

In addition, there will be a one-day Short Course on Monday June 16 which will cover "Logic Technologies for Transition from 32 nm to 22 nm". Six distinguished researchers will discuss various aspects of deeply scaled CMOS technology. The Short Course promises to be an excellent opportunity for experienced as well as new engineers to broaden their technical base.

One of the unique strengths of the Symposium on VLSI Technology has been its close association with the Symposium on VLSI Circuits. For 2008 we will expand the synergy between the Technology and Circuits communities and implement two days of overlap with a single registration fee permitting attendees to attend both technology and circuit sessions from June 17th through Jun 20th .

The symposium registration fee covers all of the sessions including the Rump Sessions, coffee breaks, Monday night Reception and the Wednesday night joint banquet for both Circuits and Technology attendees. Registration for the Short Course is extra. The registration fees and hotel reservation schedules are detailed at the end of the Advance Program.

As in past years, we expect a strong participation of top VLSI researchers from both the industry and the academic sectors. We look forward to seeing you at this year's exciting Symposium in Honolulu.

Charles Dennison	Masaaki Niwa
Program Chair	Program Co-Chair

SESSION I – TAPA I / II
Plenary Session I

Tuesday, June 17, 8:20 a.m.
Chairpersons: C. Dennison, Ovonyx, Inc.
M. Niwa, Matsushita Electric Ind. Co. Ltd.

8:20 a.m. **Welcome and Opening Remarks**
J. Woo, University of California, Los Angeles
T. Mogami, Selete

1.1 – 8:35 a.m.
Has the Sun Finally Risen on Photovoltaics?
Mark Pinto, Applied Materials

1.2 – 9:20 a.m.
Silicon Smart Microchips for Intelligent Sensing
Makoto Ishida, Toyohashi University of Technology

10:05 a.m. **Break**

SESSION 2 – TAPA I
FinFET and Multi-Gate MOSFETs

Tuesday, June 17, 10:20 a.m.
Chairpersons: W. Xiong, Texas Instruments Inc.
M. Masahara, National Institute of AIST

2.1 - 10:20 a.m.
FinFET Performance Advantage at 22nm: An AC Perspective, M. Guillorn, J. Chang, A. Bryant, N. Fuller, O. Dokumaci, X. Wang, J. Newbury, K. Babich, J. Ott, B. Haran, R. yu, C. Lavoie, D. Klaus, Y. Zhang, E. Sikorski, W. Graham, B. To, M. Lofaro, J. Tornello, D. Koli, B. Yang*, A. Pyzyna, D. Neumeyer, M. Khater, A. Yagishita**, H. Kawasaki**, W. Haensch, IBM, *AMD, **Toshiba, USA

2.2 - 10:45 a.m.
Flexible and Robust Capping-Metal Gate Integration Technology Enabling Multiple-VT CMOS in MuGFETs, A. Veloso, L. Witters, M. Demand, I. Ferain, N. J. Son, B. Kaczer. P.J. Roussel, E. Simoen, T. Kauerauf, C. Adelmann, S. Brus, O. Richard, H. Bender, T. Conard, R. Vos, R. Rooyackers, S. Van Elshocht, N. Collaert, K. De Meyer, S. Biesemans, M. Jurczak, IMEC, Belgium

2.3 - 11:10 a.m
Novel Integration Process And Performances Analysis Of Low Standby Power (LSTP) 3D Multi-Channel CMOSFET (MCFET) On SOI With Metal / High-K Gate Stack, E. Bernard, T. Ernst, B. Guillaumot*, N. Vulliet*, V. Barral, V. Maffini-Alvaro, F. Andrieu, C. Vizioz, Y. Campidelli*, P. Gautier, J.-M. Hartmann, R. Kies, V. Delaye, F. Aussenac, T. Poiroux, P. Coronel*, A. Souifi**, T. Skotnicki*, S. Deleonibus, CEA/LETI MINATEC, *STMicroelectronics, **INL-INSA Lyon, France

2.4 - 11:35 a.m.
Three-Dimensional Stress Engineering in FinFETs for Mobility/On-Current Enhancement and Gate Current Reduction, M. Saitoh, A. Kaneko, K. Okano, T. Kinoshita, S. Inaba, Y. Toyoshima, K. Uchida, Toshiba Corporation, Japan

12:00 p.m. Lunch

SESSION 3 – TAPA II
Advanced Junction Technology I

Tuesday, June 17, 10:20 a.m.
Chairpersons: O. Faynot, CEA-LETI
T. Yamashita, Renesas Technology Corp.

3.1 - 10:20 a.m.
Experimental Study of Single Source-Heterojunction MOS Transistors (SHOTs) Under Quasi-Ballistic Transport, T. Mizuno, Y. Moriyama*, T. Tezuka*, N. Sugiyama*, S. Takagi, MIRAI-AIST, *MIRAI-ASET, Japan

3.2 - 10:45 a.m.
Advanced DSS MOSFET Technology for Ultrahigh Performance Applications, M. Awano, H. Onoda, K. Miyashita, K. Adachi, Y. Kawase, K. Miyano, H. Yoshimura, T. Nakayama, Toshiba Corporation, Japan

3.3 - 11:10 a.m.
A New Source/Drain Germanium-Enrichment Process Comprising Ge Deposition and Laser-Induced Local Melting and Recrystallization for P-FET Performance Enhancement, F. Liu, H.-S. Wong, K.-W. Ang*, M. Zhu, X. Wang**, D.M.-Y. Lai^, P.-C. Lim^, B.L.H. Tan*, S. Tripathy^, S.-A. Oh^, G.S. Samudra, N. Balasubramanian*, Y.-C. Yeo, National University of Singapore, *Institute of Microelectronics, **Singapore Institute of Mfg. Technology, ^Institute of Materials Research & Eng, Singapore

3.4 - 11:35 a.m.
Novel and Cost-Efficient Single Metallic Silicide Integration Solution with Dual Schottky-Barrier Achieved by Aluminum Inter-diffusion for FinFET CMOS Technology with Enhanced Performance, R. Lee, A. Koh, W.-W. Fang, K.-M. Tan, A. Lim, T.-Y. Liow, S.-Y. Chow*, A.M. Yong*, H.S. Wong, G.-Q. Lo**, G.S. Samudra, D.-Z. Chi*, Y.-C. Yeo, National University of Singapore, *Institute of Materials Research and Engineering, **Institute of Microelectronics, Singapore

12:05 p.m. Lunch

SESSION 4 – TAPA I
Nanowire FETs

Tuesday, June 17, 1:30 p.m.
Chairpersons: T.-J. King Liu, University of California, Berkeley
S. Ohmi, Tokyo Institute of Technology

4.1 - 1:30 p.m.
Experimental Study of Mobility in [110]- and [100]-Directed Multiple Silicon Nanowire GAA MOSFETs on (100) SOI, J. Chen, T. Saraya, K. Miyaji, K. Shimizu, T. Hiramoto, University of Tokyo, Japan

4.2 - 1:55 p.m.
Performance Breakthrough in 8 nm Gate Length Gate-All-Around Nanowire Transistors using Metallic Nanowire Contacts, Y. Jiang, T.Y. Liow, N. Singh, L.H. Tan, G.Q. Lo, D.S.H. Chan*, D.L. Kwong, Institute of Microelectronics, *National University of Singapore, Singapore

4.3 - 2:20 p.m.
5 nm Gate Length Nanowire-FETs and Planar UTB-FETs with Pure Germanium Source/Drain Stressors and Laser-Free Melt-Enhanced Dopant (MeltED) Diffusion and Activation Technique, T.-Y. Liow, K.-M. Tan, R.T.P. Lee, M. Zhu, B.L.-H. Tan*, G.S. Samudra, N. Balasubramanian*, Y.-C. Yeo, National University of Singapore, *Insitute of Microelectronics, Singapore

4.4 - 2:45 p.m.
TSNWFET for SRAM Cell Application: Performance Variation and Process Dependency, S.D. Suk, Y.Y. Yeoh, M. Li, K.H. Yeo, S.-H. Kim, D.-W. Kim, D. Park, W.-S. Lee, Samsung Electronics, Korea

3:10 p.m. Break

SESSION 5 – TAPA II
High-k / Metal Gate Stack

Tuesday, June 17, 1:30 p.m.
Chairpersons: W. Mueller, Qimonda
Y. Akasaka, Tokyo Electron Ltd.

5.1 - 1:30 p.m.
Novel Vth Tuning Process for HfO_2 CMOS with Oxygen-doped TaC_x, W. Mizubayashi, K. Akiyama*, W. Wang, M. Ikeda*, K. Iwamoto*, Y. Kamimuta*, A. Hirano*, H. Ota, T. Nabatame*, A. Toriumi, MIRAI-ASRC, *MIRAI-ASET, Japan

5.2 - 1:55 p.m.
Novel Process To Pattern Selectively Dual Dielectric Capping Layers Using Soft-Mask Only, T. Schram, S. Kubicek, E. Rohr, S. Brus, C. Vrancken, S.-Z. Chang, V.S. Chang, R. Mitsuhashi, Y. Okuno, A. Akheyar, H.-J. Cho, J.C. Hooker, V. Paraschiv, R. Vos, F. Sebai, M. Ercken, P. Kelkar, A. Delabie, C. Adelmann, T. Witters, L.-A. Ragnarsson, C. Kerner, T. Chiarella, M. Aoulaiche, M.-J. Cho, T. Kauerauf, K. De Meyer, A. Lauwers, T. Hoffmann, P.P. Absil, S. Biesemans, IMEC, Belgium

5.3 - 2:20 p.m.
Single metal/single dielectric gate stack realizing triple effective workfunction for embedded memory application, K. Manabe, K. Masuzaki, T. Ogura*, T. Nakagawa, M. Saitoh, H. Sunamura, T. Tatsumi, H. Watanabe, NEC Corporation, *NEC Electronics Corporation, Japan

5.4 - 2:45 p.m.
Improved FET Characteristics By Laminate Design Optimization Of Metal Gates - Guidelines For Optimizing Metal Gate Stack Structure -, M. Kadoshima, T. Matsuki, N. Mise, M. Sato, M. Hayashi, T. Aminaka, E. Kurosawa, M. Kitajima, S. Miyazaki*, K. Shiraishi**, T. Chikyo^, K. Yamada^^, T. Aoyama, Y. Nara, Y. Ohji, Semiconductor Leading Edge Technologies Inc., *Hiroshima University, **University of Tsukuba, ^National Institute for Material Science, ^^Waseda University, Japan

3:10 p.m. Break

SESSION 6 – TAPA I
Ge MOSFETs

Tuesday, June 17, 3:25 p.m.
Chairpersons: S. Ikeda, ATDF
S. Chung, National Chiao Tung University

6.1 - 3:25 p.m.
Fundamentals And Extraction Of Velocity Saturation In Sub-100nm (110)-Si and (100)-Ge, L. Pantisano, L. Trojman, J. Mitard, B. DeJaeger, S. Severi, G. Eneman, G. Crupi, T. Hoffmann, I. Ferain, M. Meuris, M. Heyns, IMEC, Belgium

6.2 - 3:50 p.m.
Fermi-Level Depinning in Metal/Ge Schottky Junction and Its Application to Metal Source/Drain Ge NMOSFET, M. Kobayashi, A. Kinoshita, K. Saraswat, H.-S.P. Wong, Y. Nishi, Stanford University, USA

6.3 - 4:15 p.m.
The Effects Of Ge Composition And Si Cap Thickness On Hot Carrier Reliability Of Si/$Si_{1-X}Ge_x$/Si P-MOSFETS With High-K/Metal Gate, W.-Y. Loh, P. Majhi, S.-H. Lee*, J.-W. Oh, B. Sassman, C. Young, G. Bersuker, B.-J. Cho**, C.-S. Park, C.-Y. Kang, P. Kirsch, B.-H. Lee, H.R. Harris, H.-H. Tseng, R. Jammy, SEMATECH, *University of Texas, USA, **KAIST, Korea

6.4 - 4:40 p.m.
Impact of Source-to-Channel Carrier Injection Properties on Device Performance of Sub-100nm Metal Source/Drain Ge-pMOSFETs, H. Takeda, T. Yamamoto*, T. Ikezawa**, M. Kawada**, S. Takagi^, M. Hane, NEC Corporation, *MIRAI-ASET, **NEC Informatec Systems Ltd., ^MIRAI-AIST, Japan

SESSION 7 – TAPA II
High-k / Metal Gate Reliability

Tuesday, June 17, 3:25 p.m.
Chairpersons: R. Chau, Intel Corporation
K. Shibahara, Hiroshima University

7.1 - 3:25 p.m.
Low VT Metal-Gate/High-K Nmosfets - PBTI Dependence And VT Tune-Ability On La/Dy-Capping Layer Locations And Laser Annealing Conditions, S.Z. Chang*, T.Y. Hoffmann, H.Y. Yu*, M. Aoulaiche*, E. Rohr, C. Adelmann, B. Kaczer, A. Delabie, P. Favia, S. Van Elshocht, S. Kubicek, T. Scharm, T. Witters, L.-A. Ragnarsson, H.-J. Cho**, X. P. Wang, M. Mueller^, T. Chiarella, P. Absil, S. Biesemans, IMEC, *TSMC, **Samsung, ^NXP-TSMC Research Center, Belgium

7.2 - 3:50 p.m.
Impact Of The Different Nature Of Interface Defect States On The NBTI And 1/F Noise Of High-K / Metal Gate Pmosfets Between (100) And (110) Crystal Orientations, M. Sato, Y. Sugita, T. Aoyama, Y. Nara, Y. Ohji, Semiconductor Leading Edge Technologies, Japan

7.3 - 4:15 p.m.
Physical Understanding Of The Reliability Improvement Of Dual High-K Cmosfets With The Fifth Element Incorporation Into Hfsion Gate Dielectrics, M. Sato, N. Umezawa*, N. Mise, S. Kamiyama, M. Kadoshima, T. Morooka, T. Adachi*, T. Chikyow*, K. Yamabe**, K. Shiraishi**, S. Miyazaki^, A. Uedono**, K. Yamada^^, T. Aoyama, T. Takahisa, Y. Nara, Y. Ohji, Selete, *NIMS, **University of Tsukuba, ^Hiroshima University, ^^Waseda University, Japan

7.4 - 4:40 p.m.
Guidelines To Improve Mobility Performances And BTI Reliability Of Advanced High-K/Metal Gate Stacks, X. Garros, M. Casse, G. Reimbold, F. Martin, C. Leroux, A. Fanton, O. Renault, V. Cosnier*, F. Boulanger, CEA-LETI MINATEC, *STMicroelectronics, France

JOINT TECHNOLOGY/CIRCUITS RUMP SESSION
Tuesday, June 17
8:00 p.m – 10:00 p.m.

Organizers:

Technology	**Circuits**
T. Grider, Texas Instruments	G. Lehmann, Infineon
Y. Omura, Kansai University	K. Arimoto, Renesas

RJ1: Ten years after – Has SOI finally arrived?
Tapa I
Moderators: L. Counts, LC Consulting
K. Ishimaru, Toshiba America Electronic Components

Ten years after introduction of SOI into a production as a competitor to bulk-CMOS, both technologies continue to co-exist in some of the application domains, such as microprocessors and gaming. On the other hand, mainstream SoC's exclusively use bulk-CMOS. A panel similar to this one 10 years ago has concluded that SOI has a performance advantage over bulk, and the cost will be its main barrier for wide adoption. Has anything changed and will it change in the next decade? Will SOI penetrate more market segments or disappear? Does further technology scaling require the migration to fully-depleted SOI?

Panelists:

M. Bohr, Intel	R. Mahnkopf, Infineon
G. Shahidi, IBM	C. Mazure, SOITEC
E. Suzuki, AIST	D. Scott, TSMC
A. Kameyama, Toshiba	M. Usami, Hitachi

TECHNOLOGY RUMP SESSIONS
8:00 p.m. – 10:00 p.m.

R1: Who will keep SRAM scaling alive by 2012: Designers or Technologists?

Honolulu I

Moderators: K. Zhang, Intel
K. Takeuchi, NEC

Six-transistor (6T) -based SRAM has been the workhorse in all modern VLSI systems as the choice of embedded memory due to superior performance, low-power consumption, and most importantly, full compatibility with CMOS Logic technology. Scaling of the 6T SRAM has followed Moore's law faithfully over decades. But with continuous miniaturization of the SRAM cell, SRAM scaling has run into some fundamental scaling difficulties that are deeply rooted in the nature of the 6T SRAM cell itself. For example, ever-increasing transistor variation and mismatch are rapidly reducing both read stability and write margin of the cell, threatening the very existence of the operating window. This is particularly difficult when product voltage is being aggressively scaled down to meet power requirements. There has been growing concern within the VLSI design and technology community about the viability of SRAM scaling beyond the 32nm/22nm node. The search for alternatives to the 6T SRAM has already begun.

A panel of experts has been assembled from both technology and design fields to address some of the most challenging questions facing today's SRAM scaling, including:

- What will set the fundamental scaling limit for 6T SRAM?
- Will innovative new process technologies, e.g. Tri-Gate/Fin-FET, help to prolong SRAM scaling?
- Will other embedded memories such as eDRAM/ZRAM outlast or replace the SRAM?
- What circuit mitigation schemes could help save 6T SRAM scaling?
- Is it time to expand the number of transistors in the SRAM cell while keeping the area scaling competitive?

Panelists:

A. Bhavnagarwala, IBM	M. Clinton, Texas Instruments
C. Wann, TSMC	T. Furuyama, Toshiba
C. Webb, Intel	Y. Yamagata, NEC

R2: More Than Moore – Functional Diversification
Honolulu II
Moderators: T. Skotnicki, STMicroelectronics
M. Kada, ASET

In parallel to the CMOS scaling effort known as “More Moore” (MM), a new field called “More Than Moore” (MTM) has emerged recently. Whereas MM mainly focuses on computational and memory functions, MTM targets a functional diversification. The investment dedicated to MTM, and to Nano-technologies MTM employs, is probably among the highest humanity expenditures for science. The promise related with the “More Than Moore” is enormous and reaches such new functions as RF passives, sensing, actuation, acoustic, imaging, fluidics, bio-interfaces, medical, pharmaceutical, micro energy sources, and many others existing or to be invented. On the other hand the offering in terms of MTM products is still very weak on the market. Six international experts in the above mentioned fields will familiarize this Rump audience with the promises and challenges of the “More Than Moore”. We will ask their views on the key problems and difficulties they have been facing. We will ask why MTM is still so little? When it is going to be more, when it is going to launch more products on the market? We will ask them to convince the audience that “Nano” and MTM are really more than just a way to drain public money. That they are really going to repay the debt and to render humanity a huge service that no other science or technology is capable of doing. As we are mainly the CMOS community, the vital question for us is to know if MTM technologies are going to co-exist or to replace CMOS in the future? Those and many other questions from the audience and from the moderators will be discussed in an open, frank and constructive atmosphere. Feel invited!

Panelists:

M. Koyanagi, Tohoku Univ.
K. Masu, Tokyo Inst. of Tech.
T. Ning, IBM TJ Watson Res. Ctr.
H. Ishiuchi, Toshiba
M. Moussavi, CEA LITEN
S. Hillenius, SRC

CIRCUITS SESSION – TAPA II
Plenary Session

Wednesday, June 18, 8:25 a.m.
Chairpersons: K. Nakamura, Analog Devices Inc.
M. Mizuno, NEC Corporation

8:25 a.m. **Welcome and Opening Remarks**
S. Kosonocky, AMD
K. Yano, Hitachi Ltd.

1.1 – 8:40 a.m.
Next Generation Micro-Power Systems
A.P. Chandrakasan, D.C. Daly, J. Kwong, Y.K. Ramadass, Massachusetts Institute of Technology

1.2 – 9:25 a.m.
Power-Efficient Heterogeneous Parallelism for Digital Convergence
K. Uchiyama, Hitachi Ltd.

10:10 a.m. Break

SESSION 8 – TAPA I
Gate Stack Reliability

Wednesday, June 18, 8:30 a.m.
Chairpersons: M. Mueller, NXP Semiconductors
R. Yamada, Hitachi Ltd.

8.1 - 8:30 a.m.
Electron Trapping: An Unexpected Mechanism of NBTI and Its Implications, J. Campbell, K.P. Cheung, J. Suehle, A. Oates*, NIST, USA, TSMC, Taiwan

8.2 - 8:55 a.m.
I_d Fluctuations by Stochastic Single-Hole Trappings in High-*k* Dielectric p-MOSFETs, S. Kobayashi, M. Saitoh, K. Uchida, Toshiba Corporation, Japan

8.3 - 9:20 a.m.
Role Of Oxygen Vacancy In Hfo_2/Ultra-Thin SiO_2 Gate Stacks - Comprehensive Understanding Of V_{FB} Roll-Off -, K. Akiyama, W. Wang*, W. Mizubayashi*, M. Ikeda, H. Ota*, T. Nabatame, A. Toriumi*, MIRAI-ASET, *MIRAI-ASRC, Japan

8.4 - 9:45 a.m.
Mechanisms Limiting EOT Scaling and Gate Leakage Currents of High-k/Metal Gate Stacks Directly on SiGe and a Method to Enable Sub-1nm EOT, J. Huang, P.D. Kirsch, J. Oh, S.H. Lee, J. Price, P. Majhi*, H.R. Harris**, D.C. Gilmer, D.Q. Kelly, P. Sivasubramani, G. Bersuker, D. Heh, C. Young, C.S. Park, Y.N. Tan, N. Goel*, C. Park, P.Y. Hung, P. Lysaght, K.J. Choi^, B.J. Cho^^, H.-H. Tseng, B.H. Lee, R. Jammy, SEMATECH, USA, *Intel, **AMD, ^Jusung Engineering, ^^KAIST, Korea

10:10 a.m. Break

SESSION 9 – TAPA II
Highlights

Wednesday, June 18, 10:25 a.m.
Chairpersons: C. Dennison, Ovonyx, Inc.
M. Niwa, Matsushita Electric Ind. Co.

9.1 - 10:25 a.m.
Fully Integrated and Functioned 44nm DRAM Technology for 1GB DRAM, H. Lee, D.-Y. Kim, B.-H. Choi, G.-S. Cho, S.-W. Chung, W.-S. Kim, M.-S. Chang, Y.-S. Kim, J. Kim, T.-K. Kim, H.-H. Kim, H.-J. Lee, H.-S. Song, S.-K. Park, J.-W. Kim, S.-J. Hong, S.-W. Park, Hynix Semiconductor, Korea

9.2 - 10:50 a.m.
A Cost Effective 32nm High-K/ Metal Gate CMOS Technology for Low Power Applications with Single-Metal/Gate-First Process, X. Chen, S. Samavedam*, V. Narayanan, K. Stein, C. Hobbs*, C. Baiocco, W. Li, D. Jaeger, M. Zaleski*, S. Yang, N. Kim**, Y. Lee, D. Zhang*, L. Kang*, J. Chen**, H. Zhuang^, A. Sheikh, J. Wallner, M. Aquilino, J. Han^, Z. Jin, J. Li, G. Massey, S. Kalpat, R. Jha, N. Moumen, R. Mo, S. Kershnan, X. Wang, M. Chudzik, M. Chowdhury*, D. Nair, C. Reddy*, Y.W. Teh**, C. Kothandaraman, D. Coolbaugh, S. Pandey**, D. Tekleab**, A. Thean*, M. Sherony, C. Lage*, J. Sudijono**, R. Lindsay^, J.-H. Ku^^, M. Khare, A. Steegen, IBM SDRC, *Freescale Semiconductor, **Chartered Semiconductor Manufacturing, ^Infineon Technologies, ^^Samsung Electronics Co., USA

9.3 - 11:15 a.m.
Variability Aware Modeling and Characterization in Standard Cell in 45nm CMOS with Stress Enhancement Technique, H. Aikawa, E. Morifuji, T. Sanuki, T. Sawada, S. Kyoh, A. Sakata, M. Ohta, H. Yoshimura, T. Nakayama, M. Iwai, F. Matsuoka, Toshiba Corporation Semicoductor Company, Japan

9.4 - 11:40 a.m.
A Scaled Floating Body Cell (FBC) Memory with High-*k*+Metal Gate on Thin-Silicon and Thin-BOX for 16-nm Technology Node and Beyond, I. Ban, U. Avci, D. Kencke, P. Chang, Intel Corporation, USA

12:05 p.m. Lunch

SESSION 10 – TAPA I
Alternate Non Volatile Memory Technology

Wednesday, June 18, 1:30 p.m.
Chairpersons: K. Parekh, Micron
S. Ohnishi, Sharp Corporation

10.1 - 1:30 p.m.
On the Dynamic Resistance and Reliability of Phase Change Memory, B. Rajendran, M.-H. Lee*, M. Breitwisch, G. Burr, Y.-H. Shih*, R. Cheek, A. Schrott, C.-F. Chen*, M. Lamorey, E. Joseph, Y. Zhu, R. Dasaka, P. Flaitz, F. Baumann, H.-L. Lung*, C. Lam, IBM, Macronix International Co., USA

10.2 - 1:55 p.m.
Two-bit Cell Operation in Diode-Switch Phase Change Memory Cells with 90nm Technology, D.-H. Kang, J.-H Lee, J.H. Kong, D. Ha, J. Yu, C.Y. Um, J.H. Park, F. Yeung, J.H Kim, W.I. Park, Y.J Jeon, M.K. Lee, J.H. Park, Y.J. Song, J.H. Oh, G.T. Jeong, H.S. Jeong, Samsung Electronics Co., Korea

10.3 - 2:20 p.m.
A Unified Physical Model of Switching Behavior in Oxide-Based RRAM, N. Xu, B. Gao, L. Liu, B. Sun, X. Liu, R. Han, J. Kang, B. Yu*, Peking University, China, *NASA Ames Research Center, USA

10.4 - 2:45 p.m.
An Endurance-Free Ferroelectric Random Access Memory as a Non-volatile RAM, D.J. Jung, W.S. Ahn, Y.K. Hong, H.H. Kim, Y.M. Kang, J.Y. Kang, E.S. Lee, H.K. Ko, S.Y. Kim, W.W. Jung, J.H. Kim, S.K. Kang, J.Y. Jung, H.S. Kim, D.Y. Choi, S.Y. Lee, K.H. A, C. Wei, H.S. Jeong, Samsung Electronics Co., Korea

3:10 p.m. **Break**

SESSION 11 – HONOLULU SUITE
Advanced Process Technology

Wednesday, June 18, 1:30 p.m.
Chairpersons: B. van Schravendijk, Novellus Systems
Y. Igarashi, Oki Electric Industry Co. Ltd.

11.1 - 1:30 p.m.
A New Direct Low-k/Cu Dual Damascene (DD) Contact Lines for Low-loss (LL) CMOS Device Platforms, J. Kawahara, M. Ueki, M. Tagami, K. Yako, H. Yamamoto, F. Ito, H. Nagase, S. Saito, N. Furutake, T. Onodera, T. Takeuchi, H. Nakamura*, K. Arita*, K. Motoyama*, E. Nakazawa*, K. Fujii*, M. Sekine*, N. Okada*, Y. Hayashi, NEC Corporation, *NEC Electronics Corporation, Japan

11.2 - 1:55 p.m.
A Novel CVD-SiBCN Low-K Spacer Technology for High-Speed Applications, C.H. Ko, T.M. Kuan, K. Zhang*, G. Tsai*, S.M. Seutter*, C.H. Wu, T.J. Wang, C.N. Ye, H.W. Chen, C.H. Ge, K.H. Wu, W.C. Lee, Taiwan Semiconductor Manufacturing Company, Taiwan, *Applied Materials Inc., USA

11.3 - 2:20 p.m.
A Proposal of New Concept Milli-second Annealing: Flexibly-Shaped-Pulse Flash Lamp Annealing (FSP-FLA) for Fabrication of Ultra Shallow Junction with Improvement of Metal Gate High-k CMOS Performance., T. Onizawa, S. Kato, T. Aoyama, Y. Nara, Y. Ohji, Semiconductor Leading Edge Technologies, Japan

11.4 - 2:45 p.m.
Steep Channel & Halo Profiles Utilizing Boron-Diffusion-Barrier Layers (Si:C) for 32 nm Node and Beyond, A. Hokazono, H. Itokawa, N. Kusunoki, I. Mizushima, S. Inaba, S. Kawanaka, Y. Toyoshima, Toshiba Corporation, Japan

3:10 p.m. **Break**

SESSION 12 – TAPA I
NAND Flash Memory

Wednesday, June 18, 3:25 p.m.
Chairpersons: J. Lutze, SanDisk Corp.
J.-T. Moon, Samsung Electronics Co., Ltd.

12.1 - 3:25 p.m.
Scaling Evaluation of BE-SONOS NAND Flash Beyond 20 nm, H.-T. Lue, T.-H. Hsu, S.C. Lai, Y.H. Hsiao, W.C. Peng, C.W. Liao, Y.F. Huang, S.P. Hong, M.T. Wu, F.H. Hsu, N.Z. Lien, S.Y. Wang, L.W. Yang, T. Yang, K.C. Chen, K.Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co. Ltd., Taiwan

12.2 - 3:50 p.m.
Highly Scalable NAND Flash Memory with Robust Immunity to Program Disturbance Using Symetric Inversion-Type Source and Drain Structure, C.-H. Lee, J. Choi, Y. Park, C. Kang, B.-I. Choi, H. Kim, H. Oh, W.-S. Lee, Samsung Electronics Co., Korea

12.3 - 4:15 p.m.
Vertical Structure NAND Flash Array Integration with Paired FinFET Multi-bit Scheme for High-density NAND Flash Memory Application, J.-M. Koo, T.-E. Yoon, T. Lee, S. Byun, Y.-G. Jin, W. Kim, S. Kim, J. Park, J. Cho, J.-D. Choe*, C.-H. Lee*, J.J. Lee*, J.-W. Han*, Y. Kang*, S. Park*, B. Kwon*, Y.-J. Jung*, I. Yoo, Y. Park, Samsung Advanced Institute of Technology, *Samsung Electronics Co., Korea

12.4 - 4:40 p.m.
Novel 3-D Structure for Ultra High Density Flash Memory with VRAT (Vertical-Recess-Array-Transistor) and PIPE (Planarized Integration on the same PlanE), J. Kim, A.J. Hong, M. Ogawa, S. Ma, E.B. Song, Y.-S. Lin, J. Han*, U.-I. Chung*, K.L. Wang, University of California, Los Angeles, USA, *Samsung Electronics Co., Korea

SESSION 13 – HONOLULU SUITE
High-k / Metal Gate and Strain

Wednesday, June 18, 3:25 p.m.
Chairpersons: M. Khare, IBM TJ Watson Research Center
Y. Mochizuki, NEC Corporation

13.1 - 3:25 p.m.
Channel-Stress Study on Gate-Size Effects for Damascene-Gate pMOSFETs with Top-Cut Compressive Stress Liner and eSiGe, S. Mayuzumi, S. Yamakawa, D. Kosemura*, M. Takei*, J. Wang, T. Ando, Y. Tateshita, M. Tsukamoto, H. Wakabayashi, T. Ohno, A. Ogura*, N. Nagashima, Sony Corporation, *Meiji University, Japan

13.2 - 3:50 p.m.
45nm High-k + Metal Gate Strain-Enhanced Transistors, C. Auth, A. Cappellani, J.-S. Chun, A. Dalis, A. Davis, T. Ghani, G. Glass, T. Glassman, M. Harper, M. Hattendorf, P. Hentges, S. Jaloviar, S. Joshi, J. Klaus, K. Kuhn, D. Lavric, M. Lu, H. Mariappan, K. Mistry, B. Norris, N. Rahhal-Orabi, P. Ranade, J. Sandford, L. Shifren, V. Souw, K. Tone, F. Tambwe, A. Thompson, D. Towner, T. Troeger, P. Vandervoorn, C. Wallace, J. Wiedemer, C. Wiegand, Intel Corp., USA

13.3 - 4:15 p.m
Strain Enhanced Low-V_T CMOS Featuring La/Al-doped HfSiO/TaC and 10ps Invertor Delay, S. Kubicek, T. Schram, E. Rohr, V. Paraschiv, R. Vos, M. Demand, C. Adelmann, T. Witters, L. Nyns, A. Delabie, L.-A. Ragnarsson, T. Chiarella, C. Kerner, A. Mercha, B. Parvais, M. Aoulaiche, C. Ortolland, H. Yu, a. Veloso, L. Witters, R. Singanamalla, T. Kauerauf, S. Brus, C. Vrancken. V.S. Chang, S.-Z. Chang, R. Mitsuhashi, Y. Okuno, A. Akheyar, H.-J. Cho, J. Hooker, B.J. O'Sullivan, S. Van Elshocht, K. De Meyer, M. Jurczak, P. Absil, S. Biesemans, T. Hoffman, IMEC, Belgium

13.4 - 4:40 p.m.
Impact Of Tantalum Composition In Tac/Hfsion Gate Stack On Device Performance Of Aggressively Scaled CMOS Devices With SMT And Strained CESL, M. Goto, K. Tatsumura, S. Kawanaka, K. Nakajima, R. Ichihara, Y. Yoshimizu, H. Onoda, K. Nagatomo, T. Sasaki, T. Fukushima, A. Nomachi, S. Inumiya, H. Oguma, K. Miyashita, H. Harakawa, S. Inaba, T. Ishida, A. Azuma, T. Aoyama, M. Koyama, K. Eguchi, Y. Toyoshima, Toshiba Corporation, Japan

SESSION 14 – TAPA I
Trapped Charge NVM

Thursday, June 19, 8:30 a.m.
Chairpersons: K.-M. Chang, Freescale Semiconductor
J. Lee, MagnaChip Semiconductor Ltd.

14.1 - 8:30 a.m.
Embedded Split-Gate Flash Memory with Silicon Nanocrystals for 90nm and Beyond, G. Chindalore, J. Yater, H. Gasquet, M. Suhail, S.-T. Kang, C.M. Hong, N. Ellis, G. Rinkenberger, J. Shen, M. Herrick, W. Malloch, R. Syzdek, K. Baker, K.-M. Chang, Freescale Semiconductor, USA

14.2 - 8:55 a.m.
Gate-all-around Single Silicon Nanowire MOSFET with 7 nm Width for SONOS NAND Flash Memory, K.H. Yeo, K.H. Cho, M. Li, S.D. Suk, Y.-Y. Yeoh, M.-S. Kim, H. Bae, J.-M. Lee, S.-K. Sung, J. Seo, B. Park, D.-W. Kim, D. Park, W.-S. Lee, Samsung Electronics Co., Korea

14.3 - 9:20 a.m.
A Novel Junction-Free BE-SONOS NAND Flash, H.-T. Lue, E.-K. Lai, Y.H. Hsiao, S.P. Hong, M.T. Wu, F.H. Hsu, N.Z. Lien, S.Y. Wang, L.W. Yang, T. Yang, K.C. Chen, K.Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co., Taiwan

14.4 - 9:45 a.m.
Enhanced Endurance of Dual-bit SONOS NVM Cells Using the GIDL Read Method, A. Padilla, S. Lee, D. Carlton, T.-J. King Liu, University of California at Berkeley, USA

10:10 a.m. Break

SESSION 15 – HONOLULU SUITE
Advanced CMOS

Thursday, June 19, 8:30 a.m.
Chairpersons: S. Biesemans, IMEC
S. Hayashi, Matsushita Electric Ind. Co. Ltd.

15.1 - 8:30 a.m.
Planar Bulk^{+} Technology Using Tin/Hf-Based Gate Stack For Low Power Applications, G. Bidal, F. Boeuf, S. Denorme, N. Loubet, C. Laviron**, F. Leverd, S. Barnola**, T. Salvetat**, V. Cosnier, F. Martin**, M. Grosjean, P. Perreau**, D. Chanemougame, S. Haendler, M. Marin, M. Rafik, D. Fleury, C. Leyris, L. Clement, M. Sellier, S. Monfray, J. Bougueon, M.P. Samson, J.D. Chapon, P. Gouraud, G. Ghibaudo*, T. Skotnicki, STMicroelectronics, *IMEP, **CEA-LETI, France

15.2 - 8:55 a.m.
High Performance Sub-35 nm Bulk CMOS with Hybrid Gate Structures of NMOS; Dopant Confinement Layer (DCL) / PMOS; Ni-FUSI by Using Flash Lamp Anneal (FLA) in Ni-Silicidation, H. Ohta, K. Kawamura*, H. Fukutome, M. Tajima*, K. Okabe*, K. Ikeda, K. Hosaka, Y. Momiyama, S. Satoh, T. Sugii, Fujitsu Laboratories Ltd., Fujitsu Limited, Japan

15.3 - 9:20 a.m.
Cost-Effective Ni-Melt-FUSI Boosting 32-nm Node LSTP Transistors, H. Fukutome, K. Kawamura*, H. Ohta, K. Hosaka, T. Sakoda, Y. Morisaki, Y. Momiyama, Fujitsu Laboratories Ltd., *Fujitsu Limited, Japan

15.4 - 9:45 a.m.
Design and Demonstration of Very High-k (k~50) HfO_2 for Ultra-Scaled Si CMOS, S. Migita, Y. Watanabe*, H. Ota, H. Ito*, Y. Kamimuta*, T. Nabatame*, A. Toriumi, MIRAI-AIST, *MIRAI-ASET, Japan

10:10 a.m. Break

SESSION 16 – TAPA I
Variation

Thursday, June 19, 10:25 a.m.
Chairpersons: M.-R. Lin, AMD
T. Hiramoto, University of Tokyo

16.1 - 10:25 a.m.
Analyses of 5σ Vth Fluctuation in 65nm-MOSFETs Using Takeuchi Plot, T. Tsunomura, A. Nishida, F. Yano, A.T. Putra**, K. Takeuchi, S. Inaba, S. Kamohara, K. Terada*, T. Hiramoto, T. Mogami, MIRAI-Selete, *Hiroshima City University, **University of Tokyo, Japan

16.2 - 10:50 a.m.
Reduction of Vth Variation by Work Function Optimization for 45-nm Node SRAM Cell, G. Tsutsui, K. Tsunoda, N. Kariya, Y. Akiyama, T. Abe, S. Maruyama, T. Fukase, M. Suzuki, Y. Yamagata, K. Imai, NEC Electronics Corporation, Japan

16.3 - 11:15 a.m.
45nm Low-Power CMOS SoC Technology with Aggressive Reduction of Random Variation for SRAM and Analog Transistors, S. Ekbote, K. Benaissa, B. Obradovic, S. Liu, H. Shichijo, F. Hou, T. Blythe, T. Houston, S. Martin, R. Taylor, A. Singh, H. Yang, G. Baldwin, Texas Instruments, USA

16.4 - 11:40 a.m.
Understanding and Prediction of EWF Modulation Induced by Various Dopants in the Gate Stack for a Gate-First Integration Scheme, X.P. Wang, H.Y. Yu, Y.-C. Yeo*, M.-F. Li*^^, S.-Z. Chang**, H.-J. Cho^, S. Kubicek, D. Wouters, G. Groeseneken, S. Biesemans, IMEC, Belgium, *National University of Singapore, Singapore, **TSMC, ^Samsung, Taiwan, ^^Fudan University, China

12:05 p.m. Lunch

SESSION 17 – HONOLULU SUITE
Advanced SOI

Thursday, June 19, 10:25 a.m.
Chairpersons: T. Skotnicki, STMicroelectronics
T. Wakabayashi, Sony Corporation

17.1 - 10:25 a.m.
Smallest V_{th} Variability Achieved by Intrinsic Silicon on Thin BOX (SOTB) CMOS with Single Metal Gate, Y. Morita, R. Tsuchiya, T. Ishigaki, N. Sugii, T. Iwamatsu*, T. Ipposhi*, H. Oda*, Y. Inoue*, K. Torii, S. Kimura, Hitachi Ltd., *Renesas Technology Corp., Japan

17.2 - 10:50 a.m.
Selenium Co-implantation and Segregation as a New Contact Technology for Nanoscale SOI N-FETs Featuring NiSi:C Formed on Silicon-Carbon (Si:C) Source/Drain Stressors, H.-S. Wong, F.-Y. Liu, K.-W. Ang*, S.-M. Koh, A.T.-Y. Koh, T.-Y. Liow, R.T.-P. Lee, A.E.-J. Lim, W.-W. Fang, M. Zhu, L. Chan, N. Balasubramaniam*, G. Samudra, Y.-C. Yeo, National University of Singapore, *Institute of Microelectronics, Singapore

17.3 - 11:15 a.m.
Mobility Of Strained And Unstrained Short Channel FD-SOI Mosfets: New Insight By Magnetoresistance, M. Casse, F. Rochette, N. Bhouri, F. Andrieu, D.K. Maude*, M. Mouis**, G. Reimbold, F. Boulanger, CEA-LETI MINATEC, *CNRS-GHMFL, **IMEP CNRS/INPG/UJF, France

17.4 - 11:40 a.m.
On Implementation of Embedded Phosphorus-doped SiC Stressors in SOI nMOSFETs, Z. Ren, G. Pei*, J. Li, B.F. Yang*, R. Takalkar, K. Chan, G. Xia, Z. Zhu, A. Madan, T. Pinto, T. Adam, J. Miller, A. Dube, L. Black*, J.W. Weijtmans*, B. Yang*, E. Harley, A. Chakravarti, T. Kanarsky, R. Pal*, I. Lauer^, D.-G. Park^, D. Sadana^, IBM SRDC, ^IBM T.J. Watson Research Center, *AMD Inc., USA

12:05 p.m. Lunch

SESSION 18 – TAPA I
Performance Enhanced CMOS

Thursday, June 19, 1:30 p.m.
Chairpersons: K. Schruefer, Infineon Technologies
H. Kurata, Fujitsu Laboratories Ltd.

18.1 - 1:30 p.m.
A Designer Friendly 45nm High Performance Technology with In-situ C-doped e-SiGe & Dual Stress Liner in SRAM, R. Khamankar, C. Bowen, H. Bu, D. Corum, I. Fujii, B. Hornung, T. Kim, B. Kirkpatrick, K. Kirmse, A. Krishnan, C. Lin, L. Liu, T. Lowry, C. Montgomery, O. Olubuyide, S. Prins, D. Riley, S. Yu, J. Blatchford, C. Machala, C. O'Brien, G. Shin, T. Grider, Texas Instruments, USA

18.2 - 1:55 p.m.
Higher Hole Mobility Induced By Twisted Direct Silicon Bonding (DSB), M. Hamaguchi, H. Yin*, K. Saenger**, C.-Y. Sung**, R. Hasumi, R. Iijima, K. Ohuchi, Y. Takasu, J. Ott**, H. Kang*, M. Biscardi*, J. Li*, A. Domenicucci*, Z. Zhu*, P. Ronsheim*, R. Zhang*,

N. Rovedo*, H. Utomo*, K. Fogel**, J.P. De Souza**, D.K. Sadana**, M. Takayanagi, D. Park*, G. Shahidi*, K. Ishimaru, Toshiba America Electronic Components Inc., *IBM SRDC, **IBM T.J. Watson Research Center, USA

18.3 - 2:20 p.m.
32nm Device Architecture Optimization for Critical Path Speed Improvement, R. Gwoziecki, S. Kohler, F. Arnaud, STMicroelectronics, France

18.4 - 2:45 p.m.
Strain Additivity in III-V Channels for CMOSFETs Beyond 22nm Technology Node, S. Suthram, Y. Sun^, P. Majhi, I. Ok*, H. Kim*, H.R. Harris, N. Geol, S. Parthasarathy^, A. Koehler^, T. Acosta^, T. Nishida^, H.-H. Tseng, W. Tsai**, J. Lee*, R. Jammy, S.E. Thompson^, SEMATECH, *University of Texas at Austin, **Intel Corp., ^University of Florida, USA

3:10 p.m. Break

SESSION 19 – HONOLULU SUITE
Advanced Junction Technology II

Thursday, June 19, 1:30 p.m.
Chairpersons: F. Nouri, Applied Materials, Inc.
E. Morifuji, Toshiba Corp. Semiconductor Co.

19.1 - 1:30 p.m.
Laser-Annealed Junctions with Advanced CMOS Gate Stacks for 32nm Node: Perspectives on Device Performance and Manufacturability, C. Ortolland, T. Noda, T. Chiarella, S. Kubicek, C. Kerner, W. Vandervorst, A. Opdebeeck, C. Vrancken, N. Horiguchi, M. De Potter, M. Aoulaiche, E. Rosseel, S. Felch*, P. Absil, R. Schreutelkamp*, S. Biesemans, T. Hoffmann, IMEC, Belgium, *Applied Materials, USA

19.2 - 1:55 p.m.
Advanced Junction Profile Design Scheme by Low-temperature Millisecond Annealing and Co-implant for High Performance CMOS, K. Ikeda, T. Miyashita, T. Kubo*, T. Yamamoto, T. Sukegawa*, K. Okabe*, H. Ohta, Y.S. Kim, H. Nagai*, M. Nishikawa*, Y. Shimamune, A. Hatada*, Y. Hayami, K. Ohkoshi*, N. Tamura, K. Sukegawa, H. Kurata, S. Satoh, M. Kase*, T. Sugii, Fujitsu Laboratories Ltd., *Fujitsu Limited, Japan

19.3 - 2:20 p.m.
Low V_t Gate-First Al/TaN/[Ir_3Si-$HfSi_{2-x}$]/HfLaON CMOS Using Simple Laser Annealing/Reflection, C.C. Liao, A. Chin, N.C. Su*, M.-F. Li**, S.J. Wang*, National Chiao-Tung University, *National Cheng Kung University, Taiwan, **National University of Singapore, Singapore

19.4 - 2:45 p.m.
Successful Enhancement of Metal Segregation at NiSi/Si Junction through Pre-amorphization Technique, Y. Nishi, Y. Tsuchiya, A. Kinoshita, A. Hokazono, J. Koga, Toshiba Corporation, Japan

3:10 p.m. Break

SESSION 20 – TAPA I
CMOS Imager and Novel Memory

Thursday, June 19, 3:25 p.m.
Chairpersons: F. Nouri, Applied Materials Inc.
H. Wakabayashi, Sony Corporation

20.1 - 3:25 p.m.
New Global Shutter CMOS Imager with 2 Transistors per Pixel, M. Funaki, T. Shimizu, S. Orihara, H. Kawanaka, M. Kurihara, H. Sato, N. Katsumata, M. Oikawa, J. Higuchi, K. Oe, R. Kuga, K. Maki, T. Nishibata, Victor Company of Japan, Japan

20.2 - 3:50 p.m.
35-nm Gate-Length and Ultra Low-Voltage (0.45 V) Operation Bulk Thyristor-SRAM/DRAM (BT-RAM) Cell with Triple Selective Epitaxy Layers (TELs), T. Sugizaki, M. Nakamura, M. Yanagita, M. Shinohara, T. Ikuta, T. Ohchi, K. Kugimiya, S. Kanda, K. Yagami, T. Oda, Sony Corporation, Japan

20.3 - 4:15 p.m.
Band Offset FinFET-Based URAM (Unified-RAM) Built on SiC for Multi-Functioning NVM and Capacitorless 1T-DRAM, J.-W. Han, S.-W. Ryu, S. Kim, C.-J. Kim, J.-H. Ahn, S.-J. Choi, K.J. Choi*, B.J. Cho, J.S. Kim**, K.H. Kim**, G.S. Lee**, J.S. Oh**, M.H. Song**, Y.C. Park**, J.W. Kim**, Y.-K. Choi, KAIST, *Jusung Engineering, **National Nanofab Center, Korea

SESSION 21 – HONOLULU SUITE
High Mobility Devices

Thursday, June 19, 3:25 p.m.
Chairpersons: A. Lacaita, Politecnico di Milano
C. Wann, TSMC

21.1 - 3:25 p.m.

PAPER WITHDRAWN AT AUTHOR'S REQUEST

21.2 - 3:50 p.m.
Integrated Wafer-Scale Growth and Transfer of Directional Carbon Nanotubes and Misaligned-Carbon-Nanotube-Immune Logic Structures, N. Patil, A. Lin, E. Myers, H.-S.P. Wong, S. Mitra, Stanford University, USA

21.3 - 4:15 p.m.
Performance Enhancement Schemes Featuring Lattice Mismatched S/D Stressors Concurrently Realized On CMOS Platform: *e*-SiGeSn S/D For pFETS By Sn^+ Implant And Sic S/D For nFETS By C^+ Implant, G.H. Wang, E.-H. Toh, X. Wang*, D.H.L. Seng**, S. Tripathy**, T. Osipowicz, T.K. Chan, G. Samudra, Y.-C. Yeo, National University of Singapore, *Singapore Institute of Manufacturing Technology, **Institute of Materials Research and Engineering, Singapore

GENERAL INFORMATION

SCOPE OF SYMPOSIUM: The Symposium on VLSI Technology covers all aspects of VLSI technology, such as: new concepts and breakthroughs in VLSI devices and processes; new functional devices including quantum effect devices with possible VLSI

implementation; materials innovation for MOSFET and interconnect in VLSI; advanced lithography and fine patterning technologies for high density VLSI; process/device modeling of VLSI devices; packaging and reliability of VLSI devices; theories and fundamentals related to the above devices; and new concepts and technologies for VLSI manufacturing.

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Symposia Registration	
Sunday, June 15	4:00 pm – 6:00 pm
Monday, June 16	7:30 am - 5:00 pm
Tuesday, June 17	7:30 am - 5:00 pm
Wednesday, June 18	7:30 am - 5:00 pm
Thursday, June 19	8:00 am – 5:00 pm
Friday, June 20	8:00 am – 3:00 pm

VLSI TECHNOLOGY SYMPOSIUM RECEPTION: A reception will be held on Monday, June 16 from 6:00 pm to 8:00 pm on the Lagoon Green.

SYMPOSIA ON VLSI TECHNOLOGY AND VLSI CIRCUITS BANQUET: The 2008 Symposia on VLSI Technology and VLSI Circuits Banquet will be held on Wednesday, June 18 on the Lagoon Green from 7:00 pm to 9:00 pm. Banquet tickets for accompanying guests can be purchased at the Registration desk in the Palace Lounge Lobby.

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