TECHNOLOGY RUMP SESSIONS - Tuesday, June 17
8:00 p.m – 10:00 p.m.

RJ1: Ten years after – Has SOI finally arrived?
Tapa I
Moderators: L. Counts, LC Consulting
K. Ishimaru, Toshiba America Electronic Components

Ten years after introduction of SOI into a production as a competitor to bulk-CMOS, both technologies continue to co-exist in some of the application domains, such as microprocessors and gaming. On the other hand, mainstream SoC's exclusively use bulk-CMOS. A panel similar to this one 10 years ago has concluded that SOI has a performance advantage over bulk, and the cost will be its main barrier for wide adoption. Has anything changed and will it change in the next decade? Will SOI penetrate more market segments or disappear? Does further technology scaling require the migration to fully-depleted SOI?

Panelists:

M. Bohr, Intel	R. Mahnkopf, Infineon
G. Shahidi, IBM	C. Mazure, SOITEC
E. Suzuki, AIST	D. Scott, TSMC
A. Kameyama, Toshiba	M. Usami, Hitachi

R1: Who will keep SRAM scaling alive by 2012: Designers or Technologists?
Honolulu I
Moderators: K. Zhang, Intel
K. Takeuchi, NEC

Six-transistor (6T) -based SRAM has been the workhorse in all modern VLSI systems as the choice of embedded memory due to superior performance, low-power consumption, and most importantly, full compatibility with CMOS Logic technology. Scaling of the 6T SRAM has followed Moore's law faithfully over decades. But with continuous miniaturization of the SRAM cell, SRAM scaling has run into some fundamental scaling difficulties that are deeply rooted in the nature of the 6T SRAM cell itself. For example, ever-increasing transistor variation and mismatch are rapidly reducing both read stability and write margin of the cell, threatening the very existence of the operating window. This is particularly difficult when product voltage is being aggressively scaled down to meet power requirements. There has been growing concern within the VLSI design and technology community about the viability of SRAM scaling beyond the 32nm/22nm node. The search for alternatives to the 6T SRAM has already begun.

A panel of experts has been assembled from both technology and design fields to address some of the most challenging questions facing today's SRAM scaling, including:

- What will set the fundamental scaling limit for 6T SRAM?
- Will innovative new process technologies, e.g. Tri-Gate/Fin-FET, help to prolong SRAM scaling?
- Will other embedded memories such as eDRAM/ZRAM outlast or replace the SRAM?
- What circuit mitigation schemes could help save 6T SRAM scaling?
- Is it time to expand the number of transistors in the SRAM cell while keeping the area scaling competitive?

Panelists:

A. Bhavnagarwala, IBM	M. Clinton, Texas Instruments
C. Wann, TSMC	T. Furuyama, Toshiba
C. Webb, Intel	Y. Yamagata, NEC

(See R2 on next page)

R2: More Than Moore – Functional Diversification
Honolulu II
Moderators: T. Skotnicki, STMicroelectronics
M. Kada, ASET

In parallel to the CMOS scaling effort known as “More Moore” (MM), a new field called “More Than Moore” (MTM) has emerged recently. Whereas MM mainly focuses on computational and memory functions, MTM targets a functional diversification. The investment dedicated to MTM, and to Nano-technologies MTM employs, is probably among the highest humanity expenditures for science. The promise related with the “More Than Moore” is enormous and reaches such new functions as RF passives, sensing, actuation, acoustic, imaging, fluidics, bio-interfaces, medical, pharmaceutical, micro energy sources, and many others existing or to be invented. On the other hand the offering in terms of MTM products is still very weak on the market. Six international experts in the above mentioned fields will familiarize this Rump audience with the promises and challenges of the “More Than Moore”. We will ask their views on the key problems and difficulties they have been facing. We will ask why MTM is still so little? When it is going to be more, when it is going to launch more products on the market? We will ask them to convince the audience that “Nano” and MTM are really more than just a way to drain public money. That they are really going to repay the debt and to render humanity a huge service that no other science or technology is capable of doing. As we are mainly the CMOS community, the vital question for us is to know if MTM technologies are going to co-exist or to replace CMOS in the future? Those and many other questions from the audience and from the moderators will be discussed in an open, frank and constructive atmosphere. Feel invited!

Panelists:

M. Koyanagi, Tohoku Univ.
K. Masu, Tokyo Inst. of Tech.
T. Ning, IBM TJ Watson Res. Ctr.
H. Ishiuchi, Toshiba
M. Moussavi, CEA LITEN
S. Hillenius, SRC