SESSION 10 – TAPA I
Alternate Non Volatile Memory Technology

Wednesday, June 18, 1:30 p.m.
Chairpersons: K. Parekh, Micron
S. Ohnishi, Sharp Corporation

10.1 - 1:30 p.m.
On the Dynamic Resistance and Reliability of Phase Change Memory, B. Rajendran, M.-H. Lee*, M. Breitwisch, G. Burr, Y.-H. Shih*, R. Cheek, A. Schrott, C.-F. Chen*, M. Lamorey, E. Joseph, Y. Zhu, R. Dasaka, P. Flaitz, F. Baumann, H.-L. Lung*, C. Lam, IBM, Macronix International Co., USA

A novel characterization metric for phase change memory based on the measured cell resistance during RESET programming is introduced. We show that this 'dynamic resistance' (Rd) is inversely related to the programming current (I), as Rd = [A/I] + B. While the slope parameter 'A' depends only on the intrinsic properties of the phase change material, the intercept 'B' also depends on the effective physical dimensions of the memory element. We demonstrate that these two parameters provide characterization and insight into the degradation mechanisms of memory cells during operation.

10.2 - 1:55 p.m.
Two-bit Cell Operation in Diode-Switch Phase Change Memory Cells with 90nm Technology, D.-H. Kang, J.-H Lee, J.H. Kong, D. Ha, J. Yu, C.Y. Um, J.H. Park, F. Yeung, J.H Kim, W.I. Park, Y.J Jeon, M.K. Lee, J.H. Park, Y.J. Song, J.H. Oh, G.T. Jeong, H.S. Jeong, Samsung Electronics Co., Korea

This paper firstly reports key factors which are to be necessarily considered for the successful two-bit (four-level) cell operation in a phase-change random access memory (PRAM). They are 1) the write-and-verify (WAV) writing of four-level resistance states and 2) the moderate-quenched (MQ) writing of intermediate resistance levels, 3) the optimization of temporal resistance increase (so-called resistance drift) and 4) of resistance increase after thermal annealing. With taking into account of them, we realized a two-bit cell operation in diode-switch phase change memory cells with 90nm technology. All of four resistance levels are highly write endurable and immune to write disturbance above 108 cycles, respectively. In addition, they are non-destructively readable above 107 read pulses at 100ns and 1uA.

10.3 - 2:20 p.m.
A Unified Physical Model of Switching Behavior in Oxide-Based RRAM, N. Xu, B. Gao, L. Liu, B. Sun, X. Liu, R. Han, J. Kang, B. Yu*, Peking University, China, *NASA Ames Research Center, USA

Excellent bipolar resistive switching behavior was achieved in TiN/ZnO/Pt resistive random access memory (RRAM) devices. A unified physical model based on electrons hopping transport among oxygen vacancies along the conductive filaments is proposed to elucidate the resistive switching behavior in the RRAM devices. In the unified physical model, a new reset mechanism due to the depletion of electrons in oxygen vacancies and the recovery of electron-depleted oxygen vacancies with non-lattice oxygen ions is proposed and identified.

10.4 - 2:45 p.m.
An Endurance-Free Ferroelectric Random Access Memory as a Non-volatile RAM, D.J. Jung, W.S. Ahn, Y.K. Hong, H.H. Kim, Y.M. Kang, J.Y. Kang, E.S. Lee, H.K. Ko, S.Y. Kim, W.W. Jung, J.H. Kim, S.K. Kang, J.Y. Jung, H.S. Kim, D.Y. Choi, S.Y. Lee, K.H. A, C. Wei, H.S. Jeong, Samsung Electronics Co., Korea

We demonstrate endurance characteristics of a 1T1C, 64 Mb FRAM in a real-time operational situation. To explore endurance properties in address access time tAA of 100 ns, we establish a measurement set-up that covers asymmetric pulse-chains corresponding to D1- and D0-READ/RESTORE/WRITE over a frequency range from 1.0 to 7.7 MHz. What has been achieved is that endurance cycles approximate 5.9 x 1024 of cycle times in an operational condition of VDD = 2.0 V and 85 oC in the developed 64 Mb FRAM. Donor concentration due to build-up of oxygen vacancy in a ferroelectric film has also been evaluated to 2.3 x 1020 cm-3 from I-V-t measurements.