SESSION 11 – HONOLULU SUITE
Advanced Process Technology

Wednesday, June 18, 1:30 p.m.
Chairpersons: B. van Schravendijk, Novellus Systems
Y. Igarashi, Oki Electric Industry Co. Ltd.

11.1 - 1:30 p.m.
A New Direct Low-k/Cu Dual Damascene (DD) Contact Lines for Low-loss (LL) CMOS Device Platforms, J. Kawahara, M. Ueki, M. Tagami, K. Yako, H. Yamamoto, F. Ito, H. Nagase, S. Saito, N. Furutake, T. Onodera, T. Takeuchi, H. Nakamura*, K. Arita*, K. Motoyama*, E. Nakazawa*, K. Fujii*, M. Sekine*, N. Okada*, Y. Hayashi, NEC Corporation, *NEC Electronics Corporation, Japan

A new direct low-k/Cu dual damascene (DD) contact line has been developed for low loss (low parasitic capacitance and low resistance) CMOS device platforms by on-current BEOL technologies. The excellent low contact resistance is realized in the low-k pre-metal-dielectrics (PMD) with a reduced aspect ratio, achieving 5.4 Ω for 75nm Φ contact which is only 1/4 relative to a conventional W-plug. The CMOS active performance was improved with no reliability degradation, featuring in cost-effective RF/ubiquitous applications.

11.2 - 1:55 p.m.
A Novel CVD-SiBCN Low-K Spacer Technology for High-Speed Applications, C.H. Ko, T.M. Kuan, K. Zhang*, G. Tsai*, S.M. Seutter*, C.H. Wu, T.J. Wang, C.N. Ye, H.W. Chen, C.H. Ge, K.H. Wu, W.C. Lee, Taiwan Semiconductor Manufacturing Company, Taiwan, *Applied Materials Inc., USA

For the first time, we report a novel low-K spacer technology featuring CVD-SiBCN material with low dielectric constant of 5.2 and film stress of 430MPa to boost AC and DC CMOS performance. The SiBCN spacer approach in NMOS achieves 6% electron mobility improvement for long channel transistors and 11% gm,max gain for 35nm physical gate length. This novel approach can deliver up to 20% increase in CMOS ring speed. In addition, GIDL and gate leakage are improved by reduction of GF effects and device reliability is not adversely impacted. The SiBCN spacer technology has been demonstrated to be an effective solution for future high-speed CMOS applications.

11.3 - 2:20 p.m.
A Proposal of New Concept Milli-second Annealing: Flexibly-Shaped-Pulse Flash Lamp Annealing (FSP-FLA) for Fabrication of Ultra Shallow Junction with Improvement of Metal Gate High-k CMOS Performance., T. Onizawa, S. Kato, T. Aoyama, Y. Nara, Y. Ohji, Semiconductor Leading Edge Technologies, Japan

We propose the suitable milli-second annealing for metal/high-k device performance and ultra-shallow-junction fabrication: flexibly-shaped-pulse flash lamp annealing (FSP-FLA). The conventional FLA treatment on metal/high-k device degrades its electron mobility and BTI reliability. A recovery annealing treatment after FLA is most effective to recover those degradations. However, the annealing after dopant activation causes that of deactivation and diffusion. The FSP-FLA allowed us sub-10-milli-sec annealing follow activation FLA; it realizes high BTI reliability and high mobility without deactivation and diffusion.

11.4 - 2:45 p.m.
Steep Channel & Halo Profiles Utilizing Boron-Diffusion-Barrier Layers (Si:C) for 32 nm Node and Beyond, A. Hokazono, H. Itokawa, N. Kusunoki, I. Mizushima, S. Inaba, S. Kawanaka, Y. Toyoshima, Toshiba Corporation, Japan

Si:C layers under non-doped-Si epitaxial channel produces steep channel profile for 25 nm-LG nMOSFET. Applicability of Si:C layers to the channel engineering is studied for the first time in scaled device. This proposed structure has other benefits, such as the elimination of the Coulomb scattering or the acceleration of the carrier injection velocity at the source edge. Therefore, the importance of the steep channel profile has been confirmed to keep the advantage of the MOSFET scaling.