SESSION 12 – TAPA I
NAND Flash Memory

Wednesday, June 18, 3:25 p.m.
Chairpersons: J. Lutze, SanDisk Corp.
J.-T. Moon, Samsung Electronics Co., Ltd.

12.1 - 3:25 p.m.
Scaling Evaluation of BE-SONOS NAND Flash Beyond 20 nm, H.-T. Lue, T.-H. Hsu, S.C. Lai, Y.H. Hsiao, W.C. Peng, C.W. Liao, Y.F. Huang, S.P. Hong, M.T. Wu, F.H. Hsu, N.Z. Lien, S.Y. Wang, L.W. Yang, T. Yang, K.C. Chen, K.Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co. Ltd., Taiwan

We have successfully fabricated and characterized sub-30 nm and sub-20 nm BE-SONOS NAND Flash. Good device characteristics are achieved through two innovative processes: (1) a low-energy tilt-angle STI pocket implantation to suppress the STI corner edge effect, and (2) a drain offset using an additional oxide liner to improve the short-channel effect. The conventional self-boosting program-inhibit and ISPP for MLC storage are demonstrated for 20nm BE-SONOS NAND operation. Read current stability and read disturb life time are also evaluated. For the first time we have demonstrated successful data retention for "few-electron" (50-100) regime. Our results strongly suggest that BE-SONOS is a promising charge-trapping (CT) technology for NAND Flash scaling.

12.2 - 3:50 p.m.
Highly Scalable NAND Flash Memory with Robust Immunity to Program Disturbance Using Symetric Inversion-Type Source and Drain Structure, C.-H. Lee, J. Choi, Y. Park, C. Kang, B.-I. Choi, H. Kim, H. Oh, W.-S. Lee, Samsung Electronics Co., Korea

The symmetric inversion-type S/D structure has been employed for achieving available program disturbance for scaled NAND flash memory beyond sub-40nm node. The inversion S/D structure enables the channel doping to be reduced due to non-existence of n-lateral diffusion and it suppresses charge sharing between program-inhibit channels, resulting in superior program disturbance. Moreover, the cells show better current drivability in the technology node less than 50nm by more successful working of gate fringing field with smaller word-line gap, compared to those with the n-diffused S/D junction.

12.3 - 4:15 p.m.
Vertical Structure NAND Flash Array Integration with Paired FinFET Multi-bit Scheme for High-density NAND Flash Memory Application, J.-M. Koo, T.-E. Yoon, T. Lee, S. Byun, Y.-G. Jin, W. Kim, S. Kim, J. Park, J. Cho, J.-D. Choe*, C.-H. Lee*, J.J. Lee*, J.-W. Han*, Y. Kang*, S. Park*, B. Kwon*, Y.-J. Jung*, I. Yoo, Y. Park, Samsung Advanced Institute of Technology, *Samsung Electronics Co., Korea

Multi-bit Vertical Structure NAND (VsNAND) Flash memories with 32-paired FinFET cell string have been successfully integrated for the first time. Its array integration issues regarding the sub-10nm vertical structure fin could be solved by proper choices of isolation material, ion implantation, and word line patterning. VsNAND Flash array cells with TANOS (TaN/Al2O3/SiN/SiOx/Si) charge trap structure show possibilities of acceptable program/erase properties and cell Vth distribution characteristics for multi-level NAND Flash application.

12.4 - 4:40 p.m.
Novel 3-D Structure for Ultra High Density Flash Memory with VRAT (Vertical-Recess-Array-Transistor) and PIPE (Planarized Integration on the same PlanE), J. Kim, A.J. Hong, M. Ogawa, S. Ma, E.B. Song, Y.-S. Lin, J. Han*, U.-I. Chung*, K.L. Wang, University of California, Los Angeles, USA, *Samsung Electronics Co., Korea

The VRAT has been successfully developed, demonstrating 3-D integration with a unique, convenient and simple process, PIPE. The technology developed affords vertically stacked multi-layer Flash memory. Our simulation also shows that the new Z-VRAT structure will push the Flash memory density to 256Gb using the 50nm technology.