SESSION 13 – HONOLULU SUITE
High-k / Metal Gate and Strain

Wednesday, June 18, 3:25 p.m.
Chairpersons: M. Khare, IBM TJ Watson Research Center
Y. Mochizuki, NEC Corporation

13.1 - 3:25 p.m.
Channel-Stress Study on Gate-Size Effects for Damascene-Gate pMOSFETs with Top-Cut Compressive Stress Liner and eSiGe, S. Mayuzumi, S. Yamakawa, D. Kosemura*, M. Takei*, J. Wang, T. Ando, Y. Tateshita, M. Tsukamoto, H. Wakabayashi, T. Ohno, A. Ogura*, N. Nagashima, Sony Corporation, *Meiji University, Japan

Damascene gate process enhances the drivability in shorter gate length region, as compared to conventional gate 1st process for pFETs with compressive stress SiN liner and embedded SiGe. The origin of the gate length effect is investigated for the first time by using the UV-Raman spectroscopy. Moreover, the relationship between channel strain and gate width for damascene gate pFETs is analyzed and the effect is also demonstrated. It is found that channel strain is considerably enhanced in shorter gate length and narrower gate width by the combination of damascene gate process and stress enhancement techniques.

13.2 - 3:50 p.m.
45nm High-k + Metal Gate Strain-Enhanced Transistors, C. Auth, A. Cappellani, J.-S. Chun, A. Dalis, A. Davis, T. Ghani, G. Glass, T. Glassman, M. Harper, M. Hattendorf, P. Hentges, S. Jaloviar, S. Joshi, J. Klaus, K. Kuhn, D. Lavric, M. Lu, H. Mariappan, K. Mistry, B. Norris, N. Rahhal-Orabi, P. Ranade, J. Sandford, L. Shifren, V. Souw, K. Tone, F. Tambwe, A. Thompson, D. Towner, T. Troeger, P. Vandervoorn, C. Wallace, J. Wiedemer, C. Wiegand, Intel Corp., USA

Two key process features that are used to make 45nm generation metal gate + high-k gate dielectric CMOS transistors are highlighted in this paper. The first feature is the integration of stress-enhancement techniques with the dual metal-gate + high-k transistors. The second feature is the extension of 193nm dry lithography to the 45nm technology node pitches. Use of these features has enabled industry-leading transistor performance and the first high volume 45nm high-k + metal gate technology.

13.3 - 4:15 p.m
Strain Enhanced Low-V_T CMOS Featuring La/Al-doped HfSiO/TaC and 10ps Invertor Delay, S. Kubicek, T. Schram, E. Rohr, V. Paraschiv, R. Vos, M. Demand, C. Adelmann, T. Witters, L. Nyns, A. Delabie, L.-A. Ragnarsson, T. Chiarella, C. Kerner, A. Mercha, B. Parvais, M. Aoulaiche, C. Ortolland, H. Yu, a. Veloso, L. Witters, R. Singanamalla, T. Kauerauf, S. Brus, C. Vrancken. V.S. Chang, S.-Z. Chang, R. Mitsuhashi, Y. Okuno, A. Akheyar, H.-J. Cho, J. Hooker, B.J. O'Sullivan, S. Van Elshocht, K. De Meyer, M. Jurczak, P. Absil, S. Biesemans, T. Hoffman, IMEC, Belgium

A gate-first process was used to fabricate low VT (±0.25V) CMOS circuits with high performing High-k and Metal Gate transistors, showing ring oscillators with 15ps delay. Using conventional stress boosters, we demonstrate 16% and 11% performance improvement over our previous report for nMOS and pMOS, respectively [1]. The compatibility of SMT (Stress memorization technique) with High-k/Metal Gate is demonstrated for the first time. A comprehensive characterization of doped High-k films integrity, including reliability, process control and response at high frequency, is also reported for the first time.

13.4 - 4:40 p.m.
Impact Of Tantalum Composition In Tac/Hfsion Gate Stack On Device Performance Of Aggressively Scaled CMOS Devices With SMT And Strained CESL, M. Goto, K. Tatsumura, S. Kawanaka, K. Nakajima, R. Ichihara, Y. Yoshimizu, H. Onoda, K. Nagatomo, T. Sasaki, T. Fukushima, A. Nomachi, S. Inumiya, H. Oguma, K. Miyashita, H. Harakawa, S. Inaba, T. Ishida, A. Azuma, T. Aoyama, M. Koyama, K. Eguchi, Y. Toyoshima, Toshiba Corporation, Japan

We report TaCx/HfSiON gate stack CMOS device with simplified gate 1st process from the viewpoints of fixed charge generation and its impact on the device performance. Moderate MG/HK interface reaction is found to be a dominant factor to achieve device performance enhancement. By optimizing TaCx composition, fixed charge free TaCx/HfSiON device is successfully fabricated. Also, we have demonstrated that the strain effect in deeply scaled devices can be enhanced by eliminating the fixed charges in HfSiON, for the first time. Utilizing Stress Memorization Technique (SMT) and strained Contact Etch Stop Layer (CESL), Lg=35nm high performance TaCx/HfSiON devices is achieved.