SESSION 15 – HONOLULU SUITE
Advanced CMOS

Thursday, June 19, 8:30 a.m.
Chairpersons: S. Biesemans, IMEC
S. Hayashi, Matsushita Electric Ind. Co. Ltd.

15.1 - 8:30 a.m.
Planar Bulk$^+$ Technology Using Tin/Hf-Based Gate Stack For Low Power Applications, G. Bidal, F. Boeuf, S. Denorme, N. Loubet, C. Laviron**, F. Leverd, S. Barnola**, T. Salvetat**, V. Cosnier, F. Martin**, M. Grosjean, P. Perreau**, D. Chanemougame, S. Haendler, M. Marin, M. Rafik, D. Fleury, C. Leyris, L. Clement, M. Sellier, S. Monfray, J. Bougueon, M.P. Samson, J.D. Chapon, P. Gouraud, G. Ghibaudo*, T. Skotnicki, STMicroelectronics, *IMEP, **CEA-LETI, France

This work highlights the new Bulk+ technology using High-K dielectric, Single Metal Gate and Fully Depleted SON (Silicon On Nothing) channel for sub-45nm low cost applications. Thin Silicon channel (down to Tsi=8nm) and thin BOX (Tbox=15 to 25nm) are obtained using the SON process. Transistor performance (Wdesign/Lgate=90nm/40nm) at Vdd=1.1V and Ioff<2nA/µm is as high as 1298µA/µm for nMOS and 663µA/µm for pMOS. In addition, reliability, noise and 6T-SRAM bit cells down to 0.249µm² are characterized. Significant improvements with respect to conventional Bulk technology are demonstrated.

15.2 - 8:55 a.m.
High Performance Sub-35 nm Bulk CMOS with Hybrid Gate Structures of NMOS; Dopant Confinement Layer (DCL) / PMOS; Ni-FUSI by Using Flash Lamp Anneal (FLA) in Ni-Silicidation, H. Ohta, K. Kawamura*, H. Fukutome, M. Tajima*, K. Okabe*, K. Ikeda, K. Hosaka, Y. Momiyama, S. Satoh, T. Sugii, Fujitsu Laboratories Ltd., Fujitsu Limited, Japan

We applied Flash Lamp Annealing (FLA) in Ni-silicidation to our developed Dopant Confinement Layer (DCL) structure for the first time. We successfully improved the short channel effect with keeping a high drive current. For pMOSFET, Ni-FUSI was selectively formed and both effective work function control and thinner Teff are improved. On the other hand, unlike pMOS, Ni-FUSI process is not performed. Both higher activation of halo and reduction of parasitic resistance in nMOSFET are improved by the combination of DCL structure and FLA in Ni-silicidation. Consequently, the higher drive currents of 1255 / 759 µA/µm were obtained for CMOSFETs.

15.3 - 9:20 a.m.
Cost-Effective Ni-Melt-FUSI Boosting 32-nm Node LSTP Transistors, H. Fukutome, K. Kawamura*, H. Ohta, K. Hosaka, T. Sakoda, Y. Morisaki, Y. Momiyama, Fujitsu Laboratories Ltd., *Fujitsu Limited, Japan

We demonstrated for the first time that novel Ni-FUSI process using FLA (Melt-FUSI) dramatically improved both electrical characteristics and cost-benefit performance of LSTP devices. Since the Tinv was aggressively scaled (Tinv = 2.1nm) with keeping SiON-gate leakage current and increasing hole mobility twice, we achieved the record Ion of 300 µA/µm at the Ioff of 20 pA/µm for the pMOS transistor with the Lg of 45 nm at Vd of -1.2 V.

15.4 - 9:45 a.m.
Design and Demonstration of Very High-k (k~50) HfO_2 for Ultra-Scaled Si CMOS, S. Migita, Y. Watanabe*, H. Ota, H. Ito*, Y. Kamimuta*, T. Nabatame*, A. Toriumi, MIRAI-AIST, *MIRAI-ASET, Japan

We have demonstrated very high-k (k-50) HfO2 films by producing higher symmetric cubic structure without introducing any dopants. This cubic HfO2 film shows no degradation of both band gap and electron mobility in comparison with conventional HfO2. Process parameters such as ramp rate and anneal temperature are important to enhance the k-value. A possible role of oxygen vacancy in HfO2 film for the progress of structural phase transformation is discussed. Although some challenges remain to be solved, this is a dramatic progress in achieving very high-k dielectric films for ultra-scaled Si-CMOS.