SESSION 2 – TAPA I
FinFET and Multi-Gate MOSFETs

Tuesday, June 17, 10:20 a.m.
Chairpersons: W. Xiong, Texas Instruments Inc.
M. Masahara, National Institute of AIST

2.1 - 10:20 a.m.

FinFET Performance Advantage at 22nm: An AC Perspective, M. Guillorn, J. Chang, A. Bryant, N. Fuller, O. Dokumaci, X. Wang, J. Newbury, K. Babich, J. Ott, B. Haran, R. yu, C. Lavoie, D. Klaus, Y. Zhang, E. Sikorski, W. Graham, B. To, M. Lofaro, J. Tornello, D. Koli, B. Yang*, A. Pyzyna, D. Neumeyer, M. Khater, A. Yagishita**, H. Kawasaki**, W. Haensch, IBM, *AMD, **Toshiba, USA

At the 22 nm node, we estimate that superior electrostatics and reduced junction capacitance in FinFETs may provide a 13~23% reduction in delay relative to planar FETs. However, this benefit is offset by enhanced gate-to-source/drain capacitance (Cgs) in FinFETs. Here, we measure FinFET Cgs capacitance at 22nm-like dimensions and determine that, with optimization, the FinFET capacitance penalty can be limited to <6%, resulting in an overall advantage of up to 17% over a planar technology.

2.2 - 10:45 a.m.

Flexible and Robust Capping-Metal Gate Integration Technology Enabling Multiple-VT CMOS in MuGFETs, A. Veloso, L. Witters, M. Demand, I. Ferain, N. J. Son, B. Kaczer. P.J. Roussel, E. Simoen, T. Kauerauf, C. Adelmann, S. Brus, O. Richard, H. Bender, T. Conard, R. Vos, R. Rooyackers, S. Van Elshocht, N. Collaert, K. De Meyer, S. Biesemans, M. Jurczak, IMEC, Belgium

We report a comprehensive study on various capping integration options for WF engineering in MuGFET devices with TiN gate electrode: HfSiO/cap/TiN, cap/HfSiO/TiN and HfSiO/TiN/cap/TiN vs. reference deposition sequence HfSiO/TiN (cap=Al2O3, Dy2O3 or La2O3). We show: 1) low-VT values (<0.3V) are achieved for both nmos and pmos, with excellent process control and device behavior down to Lg≈50nm and WFIN≥20nm, for optimized gate stack configurations; 2) inserting a cap layer in-between TiN layers instead of HfSiO/cap/TiN leads to improved mobility, reduced CET without impacting JG, similar noise response and improved BTI behavior, with correction of the abnormal PBTI degradation seen for HfSiO/DyO/TiN.

2.3 - 11:10 a.m

Novel Integration Process And Performances Analysis Of Low Standby Power (LSTP) 3D Multi-Channel CMOSFET (MCFET) On SOI With Metal / High-K Gate Stack, E. Bernard, T. Ernst, B. Guillaumot*, N. Vulliet*, V. Barral, V. Maffini-Alvaro, F. Andrieu, C. Vizioz, Y. Campidelli*, P. Gautier, J.-M. Hartmann, R. Kies, V. Delaye, F. Aussenac, T. Poiroux, P. Coronel*, A. Souifi**, T. Skotnicki*, S. Deleonibus, CEA/LETI MINATEC, *STMicroelectronics, **INL-INSA Lyon, France

For the first time, ultra low IOFF (16.5pA/µm) and high IONN2P (2.27mA/µm and 1.32mA/µm) currents are obtained with a Multi-Channel CMOSFET (MCFET) architecture on SOI with a Metal / high-K Gate stack. This leads to the best ION/IOFF ratios ever reported: 1.4x108 (0.8x108) for 50nm n- (p-) MCFETs. We show, based on specifically developed integration process, characterization methods and analytical modeling, how those performances are obtained thanks to specific 3D MCFET features, in particular, transport properties, saturation regime and electrostatic behavior.

2.4 - 11:35 a.m.

Three-Dimensional Stress Engineering in FinFETs for Mobility/On-Current Enhancement and Gate Current Reduction, M. Saitoh, A. Kaneko, K. Okano, T. Kinoshita, S. Inaba, Y. Toyoshima, K. Uchida, Toshiba Corporation, Japan

In this paper, the first systematic study of uniaxial stress effects on mobility/on-current enhancement and gate current reduction in FinFETs is described. We demonstrate for the first time that gate current of (110) side-surface pFinFETs is largely reduced by longitudinal compressive stress due to out-of-plane mass increase. (110) n/pFinFETs are superior to (100) FinFETs in terms of higher mobility/on-current enhancement ratio by longitudinal strain and comparable/higher short-channel saturation current. Three-dimensional stress design in FinFETs including transverse and vertical stresses is proposed based on the understanding of stress effects beyond bulk piezoresistance.