SESSION 3 – TAPA II
Advanced Junction Technology I

Tuesday, June 17, 10:20 a.m.
Chairpersons: O. Faynot, CEA-LETI
T. Yamashita, Renesas Technology Corp.

3.1 - 10:20 a.m.
Experimental Study of Single Source-Heterojunction MOS Transistors (SHOTs) Under Quasi-Ballistic Transport, T. Mizuno, Y. Moriyama*, T. Tezuka*, N. Sugiyama*, S. Takagi, MIRAI-AIST, *MIRAI-ASET, Japan

We have experimentally studied the single source heterojunction MOSFETs (SHOTs) without the drain energy spike by optimizing the source heterostructures. The electron velocity enhancement of SHOTs against DHOTs and SSOIs slightly increases with decreasing the lattice temperatures. It has been experimentally demonstrated that the enhancement of the velocity injection efficiency associated with the band-offset at the source heterojunction becomes higher by reducing the scattering of electrons in lower temperature. Consequently, much higher carrier velocity is expected to be realized in SHOTs under quasi-ballistic transport, where the scattering rate of carriers is significantly suppressed.

3.2 - 10:45 a.m.
Advanced DSS MOSFET Technology for Ultrahigh Performance Applications, M. Awano, H. Onoda, K. Miyashita, K. Adachi, Y. Kawase, K. Miyano, H. Yoshimura, T. Nakayama, Toshiba Corporation, Japan

Dopant segregated Schottky MOSFET (DSS FET) is one of the key technologies which can improve the MOSFET performance thanks to reduction of external resistance and increase of carrier injection velocity. We have found that both laser spike annealing (LSA) and fluorine co-implant can reduce external resistance furthermore, which leads to boost drive currents of DSS FETs by 7% respectively. By optimizing these technologies, high drive currents of 1310μA/μm and 1080 A/μm at Ioff of 100 nA/μm are achieved at 1.0V and 0.9V respectively, without use of high-k/metal gate.

3.3 - 11:10 a.m.
A New Source/Drain Germanium-Enrichment Process Comprising Ge Deposition and Laser-Induced Local Melting and Recrystallization for P-FET Performance Enhancement, F. Liu, H.-S. Wong, K.-W. Ang*, M. Zhu, X. Wang**, D.M.-Y. Lai^, P.-C. Lim^, B.L.H. Tan*, S. Tripathy^, S.-A. Oh^, G.S. Samudra, N. Balasubramanian*, Y.-C. Yeo, National University of Singapore, *Institute of Microelectronics, **Singapore Institute of Mfg. Technology, ^Institute of Materials Research & Eng, Singapore

We report a new process technology for boosting the Ge content in SiGe source/drain (S/D) stressors to increase strain and performance levels in p-FETs. By laser-induced local melting and inter-mixing of an amorphous Ge layer with an underlying Si0.8Ge0.2 S/D region, a graded SiGe S/D stressor is formed upon recrystallization. Peak Ge content in the graded SiGe S/D is doubled over the as-grown film. For a p-FET with Ge enriched S/D, 21% and 12% IDsat enhancement at a fixed IOFF of 2x10-8 A/μm is observed over control p-FETs with Si0.8Ge0.2 S/D formed by RTA and LA, respectively.

3.4 - 11:35 a.m.
Novel and Cost-Efficient Single Metallic Silicide Integration Solution with Dual Schottky-Barrier Achieved by Aluminum Inter-diffusion for FinFET CMOS Technology with Enhanced Performance, R. Lee, A. Koh, W.-W. Fang, K.-M. Tan, A. Lim, T.-Y. Liow, S.-Y. Chow*, A.M. Yong*, H.S. Wong, G.-Q. Lo**, G.S. Samudra, D.-Z. Chi*, Y.-C. Yeo, National University of Singapore, *Institute of Materials Research and Engineering, **Institute of Microelectronics, Singapore

We have developed a novel and cost-efficient silicide integration solution to achieve a hole barrier height of 215 meV and electron barrier height of 665 meV simultaneously with a single metallic silicide based on aluminum inter-diffusion. It is proposed that aluminum diffuses into PtSi and forms an alloy, which lowers the electron barrier height of PtSi due to a change in the intrinsic PtSi workfunction. Additionally, we have integrated platinum germanosilicide with an ultra-low hole barrier height of 215 meV in P-FinFETs to provide a 21% enhancement in drive current performance, which is attributed to the 20 % reduction in series resistance. We have also ascertained the compatibility of PtSiGe with laser thermal annealing for further performance enhancement.