SESSION 4 – TAPA I
Nanowire FETs

Tuesday, June 17, 1:30 p.m.
Chairpersons: T.-J. King Liu, University of California, Berkeley
S. Ohmi, Tokyo Institute of Technology

4.1 - 1:30 p.m.
Experimental Study of Mobility in [110]- and [100]-Directed Multiple Silicon Nanowire GAA MOSFETs on (100) SOI, J. Chen, T. Saraya, K. Miyaji, K. Shimizu, T. Hiramoto, University of Tokyo, Japan

Experimental investigations of silicon nanowire mobility characteristics on (100) SOI as shrinking nanowire width to sub-10nm are reported. Accurate mobility estimations by advanced split CV method for 50~1000 nanowires are performed. For the first time, electron and hole mobility in [100]-directed nanowires are studied and compared with [110]-directed nanowires. It is shown that both electron and hole mobility decreases monotonically and electron mobility of [100]-directed nanowire tends to be comparable to that of [110] nanowire as decreasing nanowire width.

4.2 - 1:55 p.m.
Performance Breakthrough in 8 nm Gate Length Gate-All-Around Nanowire Transistors using Metallic Nanowire Contacts, Y. Jiang, T.Y. Liow, N. Singh, L.H. Tan, G.Q. Lo, D.S.H. Chan*, D.L. Kwong, Institute of Microelectronics, *National University of Singapore, Singapore

Parasitic S/D resistances in extremely scaled GAA nanowire devices can pathologically limit the device drive current performance. We demonstrate for the first time, that S/D extension dopant profile engineering together with successful integration of low resistivity metallic nanowire contacts greatly reduces parasitic resistances. This allows 8 nm gate length GAA nanowire devices in this work to attain record-high drive currents of 3740 µA/µm.

4.3 - 2:20 p.m.
5 nm Gate Length Nanowire-FETs and Planar UTB-FETs with Pure Germanium Source/Drain Stressors and Laser-Free Melt-Enhanced Dopant (MeltED) Diffusion and Activation Technique, T.-Y. Liow, K.-M. Tan, R.T.P. Lee, M. Zhu, B.L.-H. Tan*, G.S. Samudra, N. Balasubramanian*, Y.-C. Yeo, National University of Singapore, *Insitute of Microelectronics, Singapore

We report the first demonstration of pure Ge source/drain (S/D) stressors (unembedded) on the ultra-narrow or ultra-thin Si S/D regions of Nanowire-FETs and UTB-FETs, compressively straining the channels to provide up to ~100% IDsat enhancement. Devices with 5 nm gate lengths were fabricated. In addition, we report a novel Melt-Enhanced Dopant (MeltED) diffusion and activation technique to form embedded Ge S/D stressor in the S/D regions of nanowire-FETs, boosting the channel strain even further, and achieving ~125% IDsat enhancement.

4.4 - 2:45 p.m.
TSNWFET for SRAM Cell Application: Performance Variation and Process Dependency, S.D. Suk, Y.Y. Yeoh, M. Li, K.H. Yeo, S.-H. Kim, D.-W. Kim, D. Park, W.-S. Lee, Samsung Electronics, Korea

ION is increased about 25 % with the width/height (W/H) of 12/24 nm nanowire (NW) in comparison with the W/H of 12/12 nm at VG-VTH=1 V. With these results, we have successfully fabricated NW SRAM arrays with the W/H of 5/15 nm and LG of 40 nm for the first time. Static noise margin (SNM) of 325 mV is achieved at VD=1 V. NW height and gate oxide thickness dependency of n-ch twin silicon nanowire MOSFET (TSNWFET) on device variations is investigated. Line edge roughness and size variation are more critical than random dopant fluctuation in TSNWFET.