SESSION 5 – TAPA II
High-k / Metal Gate Stack

Tuesday, June 17, 1:30 p.m.
Chairpersons: W. Mueller, Qimonda
Y. Akasaka, Tokyo Electron Ltd.

5.1 - 1:30 p.m.

Novel Vth Tuning Process for HfO_2 CMOS with Oxygen-doped TaC_x, W. Mizubayashi, K. Akiyama*, W. Wang, M. Ikeda*, K. Iwamoto*, Y. Kamimuta*, A. Hirano*, H. Ota, T. Nabatame*, A. Toriumi, MIRAI-ASRC, *MIRAI-ASET, Japan

We have investigated effects of the oxygen doping into TaCx on the effective work function (Φm,eff) in TaCx/SiO2/Si and TaCx/HfO2/Si gate stacks. It has been found for the first time that the threshold voltage (Vth) is tunable within 0.5~0.6V for HfO2 MOSFETs by adjusting the oxygen content within 0~12 at. % in TaCx. Furthermore, it has been shown that unknown oxygen content in TaCx gates is a possible origin of scattering among the Φm,eff data reported.

5.2 - 1:55 p.m.

Novel Process To Pattern Selectively Dual Dielectric Capping Layers Using Soft-Mask Only, T. Schram, S. Kubicek, E. Rohr, S. Brus, C. Vrancken, S.-Z. Chang, V.S. Chang, R. Mitsuhashi, Y. Okuno, A. Akheyar, H.-J. Cho, J.C. Hooker, V. Paraschiv, R. Vos, F. Sebai, M. Ercken, P. Kelkar, A. Delabie, C. Adelmann, T. Witters, L.-A. Ragnarsson, C. Kerner, T. Chiarella, M. Aoulaiche, M.-J. Cho, T. Kauerauf, K. De Meyer, A. Lauwers, T. Hoffmann, P.P. Absil, S. Biesemans, IMEC, Belgium

We are reporting for the first time on the use of simple resist-based selective high-k dielectric capping removal processes of La2O3, Dy2O3 and Al2O3 on both HfSiO(N) and SiO2 to fabricate functional HK/MG CMOS ring oscillators with 40% fewer process steps compared to our previous report [1]. Both selective high-k removal (using wet chemistries) and resist strip processes (using NMP and APM) have been characterized physically and electrically indicating no major impact on Vt, EOT, Jg, mobility and gate dielectric integrity (PBTI, TDDB).

5.3 - 2:20 p.m.

Single metal/single dielectric gate stack realizing triple effective workfunction for embedded memory application, K. Manabe, K. Masuzaki, T. Ogura*, T. Nakagawa, M. Saitoh, H. Sunamura, T. Tatsumi, H. Watanabe, NEC Corporation, *NEC Electronics Corporation, Japan

We demonstrate midgap and band-edge effective workfunctions (EWFs) control with simple metal gate process scheme (single metal gate/single gate dielectric), using impurity-segregated NiSi2/SiON structure for embedded memory application. The application of midgap and band-edge EWF enables us to lower power consumption in SRAM and logic devices by 30% and 15% compared to poly-Si devices, respectively, due to reduced channel impurity concentration, suppressed gate depletion and high carrier mobility. These results show that NiSi2/SiON stack is one of the most promising candidates for future system on chip (SoC) devices with embedded memory.

5.4 - 2:45 p.m.

Improved FET Characteristics By Laminate Design Optimization Of Metal Gates - Guidelines For Optimizing Metal Gate Stack Structure -, M. Kadoshima, T. Matsuki, N. Mise, M. Sato, M. Hayashi, T. Aminaka, E. Kurosawa, M. Kitajima, S. Miyazaki*, K. Shiraishi**, T. Chikyo^, K. Yamada^^, T. Aoyama, Y. Nara, Y. Ohji, Semiconductor Leading Edge Technologies Inc., *Hiroshima University, **University of Tsukuba, ^National Institute for Material Science, ^^Waseda University, Japan

A laminate design technology of metal gates is proposed to improve FET characteristics regardless of EOT and gate dielectric material. The laminated metal gate structures are basically composed of low-Rs(sheet resistance) metal/WF(work-function)-lowering layer/ WFM(WF determining metal). A thin WFM (~2 nm) laminated by the Si-based WF-lowering layer such as poly-Si or TaSiN brings an additional benefit of dramatic improvements in mobility and PBTI in nFETs. A thick WFM (~10 nm) suppresses the WF-lowering in pFETs. The concept of the laminate design is indispensable for improving the performance in CMOSFETs.