SESSION 6 – TAPA I
Ge MOSFETs

Tuesday, June 17, 3:25 p.m.
Chairpersons: S. Ikeda, ATDF
S. Chung, National Chiao Tung University

6.1 - 3:25 p.m.
Fundamentals And Extraction Of Velocity Saturation In Sub-100nm (110)-Si and (100)-Ge, L. Pantisano, L. Trojman, J. Mitard, B. DeJaeger, S. Severi, G. Eneman, G. Crupi, T. Hoffmann, I. Ferain, M. Meuris, M. Heyns, IMEC, Belgium

A novel RFCV-technique is applied to directly quantify the short channel devices at high Vds, enabling parameter extraction like velocity saturation and critical field. This technique is applied to benchmark Si (110) and Si(100) as well as Ge devices. Similarities and crucial differences between short channel parameters in Si and Ge are discussed.

6.2 - 3:50 p.m.
Fermi-Level Depinning in Metal/Ge Schottky Junction and Its Application to Metal Source/Drain Ge NMOSFET, M. Kobayashi, A. Kinoshita, K. Saraswat, H.-S.P. Wong, Y. Nishi, Stanford University, USA

We successfully demonstrated Schottky barrier height modulation in metal/Ge Schottky junction by inserting an ultrathin interfacial SiN layer. The SiN layer suppressed strong Fermi level pinning in metal/Ge junction, which resulted in effective control of the Schottky barrier height. We systematically investigated its physics, for the first time, and almost zero Schottky barrier height was successfully obtained for electrons. We applied this technology to metal source/drain Ge NMOSFET and achieved low source/drain resistance.

6.3 - 4:15 p.m.
The Effects Of Ge Composition And Si Cap Thickness On Hot Carrier Reliability Of Si/$Si_{1-X}Ge_x$/Si P-MOSFETS With High-K/Metal Gate, W.-Y. Loh, P. Majhi, S.-H. Lee*, J.-W. Oh, B. Sassman, C. Young, G. Bersuker, B.-J. Cho**, C.-S. Park, C.-Y. Kang, P. Kirsch, B.-H. Lee, H.R. Harris, H.-H. Tseng, R. Jammy, SEMATECH, *University of Texas, USA, **KAIST, Korea

This paper reports on hot carrier degradation in strained Si/SiGe/Si p-MOSFETs using a novel low voltage carriers-separated current-voltage measurement. Post-stressed high-K dielectrics on SiGe p-channel shows higher interface traps located close to conduction band under channel hot carrier stressing and distributed interface trap under drain avalanche hot carrier stressing. Results show higher Ge% and thinner Si cap is preferably for hot carrier reliability with 10yrs lifetime at operating voltage of -0.85 V.

6.4 - 4:40 p.m.
Impact of Source-to-Channel Carrier Injection Properties on Device Performance of Sub-100nm Metal Source/Drain Ge-pMOSFETs, H. Takeda, T. Yamamoto*, T. Ikezawa**, M. Kawada**, S. Takagi^, M. Hane, NEC Corporation, *MIRAI-ASET, **NEC Informatec Systems Ltd., ^MIRAI-AIST, Japan

Sub-100nm metal source/drain (MSD) Ge-pMOSFETs are successfully fabricated and the device performance is analyzed from the aspect of source-to-channel carrier injection properties. Our full-band based device simulator is able to reproduce the experimental device characteristics, revealing that the low source-to-channel injected carrier density (Ns) of MSD Ge-devices could limit their source-drain current. In deep sub-100nm region, the quasi-ballistic transport nature tends to reduce the carrier velocity advantage of Ge to Si, while Ge-devices rather exhibit higher drain current than Si-ones with sufficiently high Ns condition. This Ns increase is a key to develop high-performance Ge-pMOSFETs.