SESSION 7 – TAPA II
High-k / Metal Gate Reliability

Tuesday, June 17, 3:25 p.m.
Chairpersons: R. Chau, Intel Corporation
K. Shibahara, Hiroshima University

7.1 - 3:25 p.m.
Low VT Metal-Gate/High-K Nmosfets - PBTI Dependence And VT Tune-Ability On La/Dy-Capping Layer Locations And Laser Annealing Conditions, S.Z. Chang*, T.Y. Hoffmann, H.Y. Yu*, M. Aoulaiche*, E. Rohr, C. Adelmann, B. Kaczer, A. Delabie, P. Favia, S. Van Elshocht, S. Kubicek, T. Scharm, T. Witters, L.-A. Ragnarsson, H.-J. Cho**, X. P. Wang, M. Mueller^, T. Chiarella, P. Absil, S. Biesemans, IMEC, *TSMC, **Samsung, ^NXP-TSMC Research Center, Belgium

A comprehensive study of abnormal PBTI behaviors in La/Dy-capped high-k low-VT nMOSFETs is reported. Process details in thermal budget (or dielectric intermixing) and oxygen content of the metal trigger the onset of PBTI abnormalities. The DVT shift relaxation during PBTI recovery periods is believed to be oxygen vacancies related, and can be suppressed either by reducing dielectric intermixing with lower laser powers, or by increasing oxygen concentration with TaCNO electrode. Putting La below HK results in a similar VT tune-ability with less thermal budget for intermixing with the IL (better PBTI), without loss of current drive-ability. We propose Ta2C/HK/LaO/IL + LLP anneal as an optimum nFETs stack for CMOS integration.

7.2 - 3:50 p.m.
Impact Of The Different Nature Of Interface Defect States On The NBTI And 1/F Noise Of High-K / Metal Gate Pmosfets Between (100) And (110) Crystal Orientations, M. Sato, Y. Sugita, T. Aoyama, Y. Nara, Y. Ohji, Semiconductor Leading Edge Technologies, Japan

We have clarified the difference in NBTI and 1/f noise of high-k/metal gate pMOSFETs between (110) and (100) oriented surfaces. Although the initial interface state density on (110) is higher than that on (100), the NBTI is better on the (110) surface. That is due to the different interface defect nature of interface defect states on (110) surface compared to (100). This difference has a strong impact on 1/f noise.

7.3 - 4:15 p.m.
Physical Understanding Of The Reliability Improvement Of Dual High-K Cmosfets With The Fifth Element Incorporation Into Hfsion Gate Dielectrics, M. Sato, N. Umezawa*, N. Mise, S. Kamiyama, M. Kadoshima, T. Morooka, T. Adachi*, T. Chikyow*, K. Yamabe**, K. Shiraishi**, S. Miyazaki^, A. Uedono**, K. Yamada^^, T. Aoyama, T. Takahisa, Y. Nara, Y. Ohji, Selete, *NIMS, **University of Tsukuba, ^Hiroshima University, ^^Waseda University, Japan

We clarified the impact of the incorporation of the fifth material into HfSiON technology for Vth control on the reliability of high-k/metal gate stacks CMOSFETs. HfMgSiON is remarkably effective for suppressing electron traps, giving rise to a dramatic PBTI lifetime improvement for nMOSFETs. With pMOSFETs, Al incorporation is effective for the thermal deactivation of hole traps, resulting in NBTI lifetime improvement. We have established the guidelines of material selection to be incorporated into HfSiON for reliability improvement for nMOS and pMOS individually.

7.4 - 4:40 p.m.
Guidelines To Improve Mobility Performances And BTI Reliability Of Advanced High-K/Metal Gate Stacks, X. Garros, M. Casse, G. Reimbold, F. Martin, C. Leroux, A. Fanton, O. Renault, V. Cosnier*, F. Boulanger, CEA-LETI MINATEC, *STMicroelectronics, France

A systematic study of mobility performances and BTI reliability was done in dielectrics stacks. By studying a large variety of dielectric stacks we also clearly demonstrate that mobility performances, interface defects Nit and NBTI reliability are strongly correlated. All are affected by nitrogen species N which is clearly identified as the main mobility killer when it reaches unintentionally the Si interface during the deposition of nitrided gates or the nitridation steps. However, by optimizing the gate stacks, excellent mobility performances, up to 100% universal mobility at Eeff=1MV/cm, and reliability can be achieved.