SESSION 8 – TAPA I
Gate Stack Reliability

Wednesday, June 18, 8:30 a.m.
Chairpersons: M. Mueller, NXP Semiconductors
R. Yamada, Hitachi Ltd.

8.1 - 8:30 a.m.
Electron Trapping: An Unexpected Mechanism of NBTI and Its Implications, J. Campbell, K.P. Cheung, J. Suehle, A. Oates*, NIST, USA, TSMC, Taiwan

We utilize fast-IdVg measurements to examine NBTI recovery over a time scale of 2usecs to 1000 seconds. The extracted VTH shift and %GM degradation data clearly demonstrates the presence of hole as well as electron trapping and detrapping. The hole and electron trapping/detrapping behavior is only observable for very fast measurement times (<10usecs) and has significant implications to the current understanding of the NBTI phenomenon and consequent lifetime predictions.

8.2 - 8:55 a.m.
I_d Fluctuations by Stochastic Single-Hole Trappings in High-*k* Dielectric p-MOSFETs, S. Kobayashi, M. Saitoh, K. Uchida, Toshiba Corporation, Japan

Random telegraph noise (RTN) in scaled FETs is one of the biggest concerns in the present and future LSIs. However, RTN in high-k gate dielectric FETs have not been fully studied yet. In this paper, we have studied RTN in high-k pFETs in comparison with that in SiO2 pFETs. It is found for the first time that the RTN amplitude (Id fluctuations) in high-k pFETs are less reduced by the surface holes, comparing to the SiO2 pFETs. It is also found that slower traps in the high-k gate dielectric more severely reduce Id.

8.3 - 9:20 a.m.
Role Of Oxygen Vacancy In Hfo_2/Ultra-Thin SiO_2 Gate Stacks - Comprehensive Understanding Of V_{FB} Roll-Off -, K. Akiyama, W. Wang*, W. Mizubayashi*, M. Ikeda, H. Ota*, T. Nabatame, A. Toriumi*, MIRAI-ASET, *MIRAI-ASRC, Japan

We report a role of the oxygen vacancy in HfO2/interfacial layer(IL-) SiO2, focusing on VFB roll-off. It is found for the first time that VFB roll-off is eliminated by inserting 1~2nm thin SiO2 (top-SiO2) between metal gate and HfO2. This roll-off elimination is explained by compensating the bottom dipoles at HfO2/IL-SiO2 interface with the counter dipoles at top-SiO2/HfO2 interface. It is concluded that the bottom dipole is assigned to the dominant origin of VFB roll-off.

8.4 - 9:45 a.m.
Mechanisms Limiting EOT Scaling and Gate Leakage Currents of High-k/Metal Gate Stacks Directly on SiGe and a Method to Enable Sub-1nm EOT, J. Huang, P.D. Kirsch, J. Oh, S.H. Lee, J. Price, P. Majhi*, H.R. Harris**, D.C. Gilmer, D.Q. Kelly, P. Sivasubramani, G. Bersuker, D. Heh, C. Young, C.S. Park, Y.N. Tan, N. Goel*, C. Park, P.Y. Hung, P. Lysaght, K.J. Choi^, B.J. Cho^^, H.-H. Tseng, B.H. Lee, R. Jammy, SEMATECH, USA, *Intel, **AMD, ^Jusung Engineering, ^^KAIST, Korea

The mechanisms of high gate leakage current in MG/HfSiON/SiGe stacks are 1) Ge enhanced Si oxidation and 2) Ge up-diffusion, the first being the primary mechanism. Optimized plasma nitridation of HfSiON/SiGe stacks addresses O and Ge diffusion issues enabling EOT=0.91nm. Dielectric deposition directly on SiGe reduces process and device design complexity associated with the common Si cap approach. This scaling and performance demonstration paves the way for surface channel SiGe pFETs at sub 32nm nodes.