SESSION 9 – TAPA II
Highlights

Wednesday, June 18, 10:25 a.m.
Chairpersons: C. Dennison, Ovonyx, Inc.
M. Niwa, Matsushita Electric Ind. Co.

9.1 - 10:25 a.m.

Fully Integrated and Functioned 44nm DRAM Technology for 1GB DRAM, H. Lee, D.-Y. Kim, B.-H. Choi, G.-S. Cho, S.-W. Chung, W.-S. Kim, M.-S. Chang, Y.-S. Kim, J. Kim, T.-K. Kim, H.-H. Kim, H.-J. Lee, H.-S. Song, S.-K. Park, J.-W. Kim, S.-J. Hong, S.-W. Park, Hynix Semiconductor, Korea

44nm feature sized 8F2 1Gb DRAM is fully integrated and functioned for the first time with the smallest cell size of 0.015um2. A novel cell-transistor structure and new DRAM process technologies are developed. In order to control the threshold voltage uniformity and body-bias sensitivity of saddle-fin cell-transistor, the channel doping profile and saddle-fin geometric dependency were analytically expressed with experimental data. The weak fin height dependency on cell-VT diminishes the burden of the saddle-fin patterning processes. And the low body-bias sensitivity of the saddle-fin cell-transistor leads wide tWR (write recovery time) margins. Cylinder-like MIM cell capacitor with ZAZ dielectric is exploited on cell capacitor. Copper implemented triple-metal layer and WN barrier-metal techniques were developed to decrease chip size.

9.2 - 10:50 a.m.

A Cost Effective 32nm High-K/ Metal Gate CMOS Technology for Low Power Applications with Single-Metal/Gate-First Process, X. Chen, S. Samavedam*, V. Narayanan, K. Stein, C. Hobbs*, C. Baiocco, W. Li, D. Jaeger, M. Zaleski*, S. Yang, N. Kim**, Y. Lee, D. Zhang*, L. Kang*, J. Chen**, H. Zhuang^, A. Sheikh, J. Wallner, M. Aquilino, J. Han^, Z. Jin, J. Li, G. Massey, S. Kalpat, R. Jha, N. Moumen, R. Mo, S. Kershnan, X. Wang, M. Chudzik, M. Chowdhury*, D. Nair, C. Reddy*, Y.W. Teh**, C. Kothandaraman, D. Coolbaugh, S. Pandey**, D. Tekleab**, A. Thean*, M. Sherony, C. Lage*, J. Sudijono**, R. Lindsay^, J.-H. Ku^^, M. Khare, A. Steegen, IBM SDRC, *Freescale Semiconductor, **Chartered Semiconductor Manufacturing, ^Infineon Technologies, ^^Samsung Electronics Co., USA

For the first time, we have demonstrated a 32nm high-k/metal gate (HK-MG) low power CMOS platform technology with low standby leakage transistors and functional high-density SRAM with a cell size of 0.157 µm2. Record NMOS/PMOS drive currents of 1000/575 µA/µm, respectively, have been achieved at 1 nA/µm off-current and 1.1V Vdd with a low cost process. With this high performance transistor, Vdd can be further scaled to 1.0V for active power reduction. Compared to SiON-Poly, 30% RO delay reduction has been demonstrated with HK-MG devices. 40% Vt mismatch reduction has been shown with the Tinv scaling. Furthermore, it has been shown that the 1/f noise and transistor reliability exceed the technology requirements.

9.3 - 11:15 a.m.

Variability Aware Modeling and Characterization in Standard Cell in 45nm CMOS with Stress Enhancement Technique, H. Aikawa, E. Morifuji, T. Sanuki, T. Sawada, S. Kyoh, A. Sakata, M. Ohta, H. Yoshimura, T. Nakayama, M. Iwai, F. Matsuoka, Toshiba Corporation Semicoductor Company, Japan

Gate density is ultimately increased to 2100 kGates/mm2 by pushing the critical design rules without increasing the circuit margin in 45nm technology. Layout dependences for stress enhanced MOSFET including contact positioning, 2nd neighboring poly effect, and bent diffusion are accurately modeled. With the constructed design flow, gate length change of -2.8% to +3.6% and Idsat change of -10% to +14% are removed from uncertain margin in 45 nm corner libraries.

9.4 - 11:40 a.m.

A Scaled Floating Body Cell (FBC) Memory with High-*k*+Metal Gate on Thin-Silicon and Thin-BOX for 16-nm Technology Node and Beyond, I. Ban, U. Avci, D. Kencke, P. Chang, Intel Corporation, USA

A scaled, undoped, thin-BOX, planar FBC technology is demonstrated for the first time, featuring 10-nm BOX, 25-nm SOI, high-k, metal gate, separate back-gate (BG) doping, and raised source-drain epitaxy. Retention of a minimum 3-microAmp sensing window for 100 ms, in devices with 60-nm gate-length (Lg) and 70-nm diffusion width (W), represents the best retention time of all sub-100-nm FBC devices. FBC scaling is predicted to be feasible at least to 40-nm Lg, enabling memory cell sizes much smaller than 6T-SRAM at 16-nm technology node. Functional 32-nm Lg devices suggest the feasibility at the 11-nm technology node.