2010 VLSI Circuits Short Course

Short Course Program 1
Circuit Design for Technology Challenges

Honolulu I
Tuesday, June 15, 8:30 a.m.

Organizers/Chairs: A. Bhavnagarwala, IBM TJ Watson Research
K. Nose, Renesas Electronics Corp.

8:30 a.m. **Introduction**
Azeez. Bhavnagarwala, IBM TJ Watson Research

8:45 a.m. **CMOS Technology Trends**
Ghavam Shahidi, IBM TJ Watson Research

9:45 a.m. **CMOS Logic and Embedded Memory Design**
Kevin Zhang, Intel

10:45 a.m. **Break**

11:00 a.m. **Design Methodology and Tools in an Evolving CMOS Technology**
Clive Bittlestone, Texas Instruments

12:00 p.m. **Lunch**

1:00 p.m. **Analog/Mixed Signal Design in Digital CMOS**
David Fishette, AMD

2:00 p.m. **Chip-Package-Co-Design**
Atsushi Nakamura, Renesas

3:00 p.m. **Break**

3:15 p.m. **Memory Design**
a. Low Power DRAM Circuits and Interface Design,
Yasuhiro Takai, Elpida Memory
b. Disturbance and interference Issues in NAND Flash Design
Ki-Tae Park, Samsung

5:00 p.m. **Conclusion**
Koichi Nose, Renesas Electronics Corp.

Short Course Program 2
Frequency Synthesis and Clock Generation

Honolulu II
Tuesday, June 15, 8:30 a.m.

Organizers/Chairs: A. Cathelin, STMicroelectronics
S. Mutoh, NTT Corp.

8:30 a.m. **Introduction**
Andreia Cathelin, STMicroelectronics

8:45 a.m. **Basics of Jitter and Phase Noise**
Asad Abidi, UCLA

9:45 a.m. **Modeling/Simulation of Large Signal Phenomena in PLL**
Rick Poore, Agilent EEs of EDA

10:45 a.m. **Break**

11:00 a.m. **Architecture Trends and Requirements for Wireless RF PLLs**
Chih-Ming Hung, Texas Instruments

12:00 p.m. **Lunch**

1:00 p.m. **Low Power Frequency Synthesis Using BAW/IC Integration**
Brian Otis, University of Washington

2:00 p.m. **Clocking Techniques for High-speed Wireline**
Jae-Yoon Sim, POSTECH

3:00 p.m. **Break**

3:15 p.m. **Mm-wave PLL Design**
Toshiya Mitomo, Toshiba Corp.

4:15 p.m. **Round Table (all the speakers)**
Shin'ichiro Mutoh, NTT Corp.

5:00 p.m. **Conclusion**

Welcome to the 2010 Symposium on VLSI Circuits

You are cordially invited to attend the 2010 Symposium on VLSI Circuits, to be held on June 16-18, 2010, at the Hilton Hawaiian Village in Honolulu, Hawaii. Following the rich tradition, the Symposium on VLSI Circuits will follow the Symposium on VLSI Technology at the same location.

Once again, the Circuits Symposium will overlap the Technology Symposium by two full days. The two overlap days between Technology and Circuits will allow attendees to freely choose to attend papers from either Symposium, providing a unique opportunity to learn about the latest advances in both VLSI Circuits and Technology, and to interact and exchange ideas with attendees from both Symposia.

The Symposium on VLSI Circuits has established itself as a major international forum for presenting and exchanging important ideas and new developments in VLSI circuit design. The scope of the conference includes new concepts in VLSI, Memory technologies, Analog Circuits, Data Converters, Digital Processing, Static and Dynamic Memory, I/O, and Wireless and Wireline Communication Circuits. Contributions to the Symposium come from both industry and academia, from around the world. This year, the circuits symposium technical program will focus on "**Looking to the Next Decade of Electronics**" as we consider the changing landscape and challenges in the semiconductor industry over the coming years

Preceding the Symposium on June 15th, two all-day Short Courses on VLSI circuits will be held. For one registration fee, participants can attend either parallel course. The first course, focusing on new challenges facing memory and digital designers is titled; "Circuit Design for Technology Challenges". The other course focuses on the increasing challenges of system integration for both analog and digital designers and is titled; "Frequency Synthesis and Clock Generation."

This year, the technical program committee reviewed 409 papers, selecting 90 outstanding papers for presentation at the Circuits Symposium. These papers disclose new and interesting design concepts for memory, processor, communication, analog, data conversion, and signal processing circuits, and represent the leading edge of VLSI circuit design. These are in addition to 89 papers selected for presentation at the Technology Symposium.

We have invited two distinguished speakers to describe recent advances and new challenges related to VLSI circuits, technology and applications: ""Opportunities in Energy Storage Due to the Paradigm Shift Fueled by the Mobile and Clean Tech Revolutions" by Dr. Christina Lampe-Önnerud of Boston-Power, Inc and "Three-Dimensional Imaging Technology: A Revolution in the World of Imaging" by Dr. Satoru Fujikawa of Panasonic Corp.

To complement the formal talks, we have arranged three evening rump sessions on interesting and provocative subjects to give you an opportunity to participate in the discussions and mix with the industry and academic experts providing their viewpoints on important topics related to the next decade of electronics. The rump sessions explore: "The Next Decade of VLSI Technology and Circuits – Are We on the Same Road?"; "A Role for VLSI in Green Technology?"; "Mixed Signal IP – Make vs. Buy".

The rich technical content of the program will undoubtedly interest you, and we certainly hope that the Symposium will be a fruitful and enjoyable experience. We look forward to meeting with you at the Symposium in Honolulu.

Ajith Amerasekera	Makoto Nagata
Program Chair	Program Co-Chair

SESSION I – TAPA II
Plenary Session

Wednesday, June 16, 8:05 a.m.
Chairpersons: A. Amerasekera, Texas Instruments
M. Nagata, Kobe University

8:05 a.m. Welcome and Opening Remarks
K. Nakamura, Analog Devices
M. Mizuno, Renesas Electronics Corp.

1.1 - 8:35 a.m.
Opportunities in Energy Storage Due to the Paradigm Shift Fueled by the Mobile and Clean Tech Revolutions, Christina Lampe-Önnerud, Boston-Power, Inc.

1.2 - 9:20 a.m.
Three-dimensional Imaging Technology: A Revolution in the World of Imaging, Satoru Fujikawa, Panasonic Corp.

SESSION 2 – TAPA I
Medical and Vision Processors

Wednesday, June 16, 10:25 a.m.
Chairperson: C. Sechen, University of Texas at Dallas
K. Kobayashi, Kyoto Institute of Technology

2.1 - 10:25 a.m.
Microwatt Embedded Processor Platform for Medical System-on-Chip Applications, S. Sridhara, M. DiRenzo, S. Lingam, S.-J. Lee, R. Blazquez, J. Maxey, S. Ghanem*, Y.-H. Lee*, R. Abdallah*, P. Singh**, M. Goel, Texas Instruments, *University of Illinois at Urbana-Champaign, **University of Michigan at Ann Arbor, USA

2.2 - 10:50 a.m.
A 1.2mW On-Line Learning Mixed Mode Intelligent Inference Engine for Robust Object Recognition, J. Oh, S. Lee, M. Kim, J. Kwon, J. Park, J.-Y. Kim, H.-J. Yoo, KAIST, Korea

2.3 - 11:15 a.m.
A Low Power ECG Signal Processor for Ambulatory Arrhythmia Monitoring System, H. Kim, R.F. Yazicioglu, T. Torfs, P. Merken, H.-J. Yoo*, C. Van Hoof, IMEC, Belgium, *KAIST, Korea

2.4 - 11:40 a.m.
1.4μW/Channel 16-Channel EEG/ECoG Processor for Smart Brain Sensor SoC, T.-C. Chen, T.-H. Lee, Y.-H. Chen, T.-C. Ma, T.-D. Chuang, C.-J. Chou, C.-H. Yang, T.-H. Lin, L.-G. Chen, National Taiwan University, Taiwan

SESSION 3 – HONOLULU SUITE
UWB Circuits

Wednesday, June 16, 10:25 a.m.
Chairperson: A. Cathelin, STMicroelectronics
J. Lee, National Taiwan University

3.1 - 10:25 a.m.
A 112Mb/s Full Duplex Remotely-Powered Impulse-UWB RFID Transceiver for Wireless NV-Memory Applications, M. Pelissier, B. Gomez, G. Masson, S. Dia, M. Gary, J. Jantunen*, J. Arponen*, J. Vartera*, CEA-LETI - Minatec, France, *Nokia, Finland

3.2 - 10:50 a.m.
A Charge-Domain Auto- and Cross-Correlation Based IR-UWB Receiver with Power- and Area-Efficient PLL for 62.5ps Step Data Synchronization in 65nm CMOS, L. Liu, T. Sakurai, M. Takamiya, University of Tokyo, Japan

3.3 - 11:15 a.m.
A 2.4GHz Wireless Transceiver with 0.95nJ/b Link Energy for Multi-Hop Battery-Free Wireless Sensor Networks, J. Ayers, N. Panitantum, K. Mayaram, T. Fiez, Oregon State University, USA

3.4 - 11:40 a.m.
A Fully Integrated, 300pJ/b, Dual Mode 65nm CMOS Transceiver for cm-Range Wireless Links, S. Gambini, J. Crossely, E. Alon, J. Rabaey, University of California, Berkeley, USA

SESSION 4 – TAPA I
SRAM Variability

Wednesday, June 16, 1:30 p.m.
Chairperson: M. Whately, Cypress Semiconductor
H. Yamauchi, Fukuoka Institute of Technology

4.1 - 1:30 p.m.
Dynamic SRAM Stability Characterization in 45nm CMOS, S.O. Toh, Z. Guo, B. Nikolic, University of California, Berkeley, USA

4.2 - 1:55 p.m.
Small-Defect Detection in Sub-100nm SRAM Cells using WL-Pulse Timing-Margin Measurement Scheme, Y. Morita, K. Nose, K. Noguchi, S. Takami*, K. Goto*, S. Aimoto*, A. Kimura*, M. Mizuno, NEC Corporation, Japan, *NEC Electronics Corporataion, Japan

4.3 - 2:20 p.m.
Tunable Replica Bits for Dynamic Variation Tolerance in 8T SRAM, A. Raychowdhury, B. Gueskens, K. Bowman, J. Tschanz, S.-L. Lu, T. Karnik, M. Khellah, V. De, Intel Corp, USA

4.4 - 2:45 p.m.
70% Read Margin Enhancement by V_{TH} Mismatch Self-Repair in 6T-SRAM with Asymmetric Pass Gate Transistor by Zero Additional Cost, Post-Process, Local Electron Injection, K. Miyaji, S. Tanakamaru, K. Honda, S. Miyano*, K. Takeuchi, University of Tokyo, Japan, *Semiconductor Technology Academic Research Center (STARC), Japan

SESSION 5 – HONOLULU SUITE
Clocking Building Blocks

Wednesday, June 16, 1:30 p.m.
Chairperson: K. Chang, Rambus, Inc.
M. Takamiya, University of Tokyo

5.1 - 1:30 p.m.
A Programmable Phase Rotator Based on Time-Modulated Injection-Locking, F. O'Mahony, B. Casper, M. Mansuri, M. Hossain*, Intel Corp, USA *University of Toronto, Canada

5.2 - 1:55 p.m.
A 5-20GHz Tunable LC-VCO Using Variable Bridge Inductor, A. Tanabe, K. Hijioka, H. Nagase, Y. Hayashi, NEC Electronics Corp, Japan

5.3 - 2:20 p.m.
A 198.9GHz-to-201.0GHz Injection-Locked Frequency Divider in 65nm CMOS, B.-Y. Lin, I.-T. Lee, C.-H. Wang, S.-I. Liu, National Taiwan University, Taiwan

5.4 - 2:45 p.m.
10MHz to 7GHz Quadrature Signal Generation Using a Divide-by-4/3, -3/2, -5/3, -2, -5/2, -3, -4, and -5 Injection-Locked Frequency Divider, S. Hara, K. Okada, A. Matsuzawa, Tokyo Institute of Technology, Japan

SESSION 6 – TAPA I
Analog Circuits

Wednesday, June 16, 3:25 p.m.
Chairperson: G. van der Plas, IMEC
M. Ito, Renesas Electronics Corp.

6.1 - 3:25 p.m.
A Fully-Integrated Switched-Capacitor 2:1 Voltage Converter with Regulation Capability and 90% Efficiency at 2.3A/mm^2, L. Chang, R. Montoye, B. Ji, A. Weger, K. Stawiasz, R. Dennard, IBM T.J. Watson Research Center, USA

6.2 - 3:50 p.m.
An Interleaving Energy-Conservation Mode (IECM) Control in Single-Inductor Dual-Output (SIDO) Step-Down Converters with 91% Peak Efficiency, Y.-H. Lee, K.-H. Chen, Y.-H. Lin*, Y.-Y. Yang, S.-J. Wang, Y.-K. Chen*, C.-C. Huang*, National Chiao Tung University, Taiwan, *Realtek Semiconductor Corp., Taiwan

6.3 - 4:15 p.m.
High Efficiency Single-Inductor Boost/Buck Inverting Flyback Converter with Hybrid Energy Transfer Media and Multi Level Gate Driving for AM OLED Panel, S.-W. Wang, Y.-J. Woo, S.-S. Yuk, G.-H. Cho, G.-H. Cho*, KAIST, Korea, *JDA Technology, Korea

6.4 - 4:40 p.m.
A High-Efficiency 4x45W Car Audio Power Amplifier using Load Current Sharing, C. Mensink, E. van Tuijl**, S. Gierkink, F. Mostert*, R. van der Zee**, Axiom IC, *NXP, **University of Twente, The Netherlands

6.5 - 5:05 p.m.
An Energy Management IC for Bio-Implants Using Ultracapacitors for Energy Storage, W. Sanchez, C. Sodini, J. Dawson, Massachussetts Institute of Technology, USA

SESSION 7 – HONOLULU SUITE
Advanced Tranceivers Techniques

Wednesday, June 16, 3:25 p.m.
Chairperson: J. Lloyd, Analog Devices
M. Igarashi, Sony Corp.

7.1 - 3:25 p.m.
An Ultra-Wide Range Bi-Directional Transceiver with Adaptive Power Control Using Background Replica VCO Gain Calibration, T. Ebuchi, Y. Komatsu, M. Miura, T. Chiba, T. Iwata, S. Dosho, T. Yoshikawa, Panasonic Corporation, Japan

7.2 - 3:50 p.m.
A 5Gb/s Speculative DFE for 2x Blind ADC-Based Receivers in 65-nm CMOS, S. Sarvari, T. Tahmoureszadeh, A. Sheikholeslami, H. Tamura*, M. Kibune*, University of Toronto, Canada, *Fujitsu Laboratories Limited, Japan

7.3 - 4:15 p.m.
A 5Gb/s Automatic Sub-Bit Between-Pair Skew Compensator for Parallel Data Communications in 0.13µm CMOS, Y. Zheng, J. Liu*, R. Payne, M. Morgan, H. Lee*, Texas Instruments, Inc., *University of Texas at Dallas, USA

7.4 - 4:40 p.m.
FDM-based Wireless Source Synchronous 15-Mbps TRx with PLL-less Receiver and 1-mm On-chip Integrated Antenna for 1.25-cm Touch-and-Proceed Communication, H. Ishizaki, T. Araki*, S. Takahashi, J. Ryu*, S. Uchida**, N. Yoshida, M. Takamiya*, M. Mizuno, NEC Corporation, Japan, *The University of Tokyo, Japan, **NEC Electronics Corporatio, Japan

7.5 - 5:05 p.m.
A 5Gb/s Link with Clock Edge Matching and Embedded Common Mode Clock for Low Power Interfaces, J. Zerbe, B. Daly, L. Luo, B. Stonecypher, W. Dettloff, J. Eble, T. Stone, J. Ren, B. Leibowitz, M. Bucher, P. Satarzadeh, Q. Lin, Rambus Inc, USA

SESSION 8 – TAPA I
High Speed On-Die Network and Processor Clocking

Thursday, June 17, 8:30 a.m.
Chairperson: S. Tam, Intel Corporation
K. Nose, Renesas Electronics Corp.

8.1 - 8:30 a.m.
A 2Tb/s 6×4 Mesh Network with DVFS and 2.3Tb/s/W router in 45nm CMOS, P. Salihundam, S. Jain, T. Jacob, S. Kumar, V. Erraguntla, Y. Hoskote, S. Vangal, G. Ruhl, P. Kundu, N. Borkar, Intel Corporation

8.2 - 8:55 a.m.
A 1.07 Tbit/s 128×128 Swizzle Network for SIMD Processors, S. Satpathy, Z. Foo, B. Giridhar, D. Sylvester, T. Mudge, D. Blaauw, University of Michigan, USA

8.3 - 9:20 a.m.
A Scalable, Sub-1W, Sub-10ps Clock Skew, Global Clock Distribution Architecture for Intel® Core™ i7/i5/i3 Microprocessors, G. Shamanna, N. Kurd, J. Douglas, M. Morrise, Intel Corporation, USA

8.4 - 9:45 a.m.
A DPLL-based per Core Variable Frequency Clock Generator for an Eight-Core POWER7™ Microprocessor, J. Tierno, A. Rylyakov, D. Friedman, A. Chen, A. Ciesla, T. Diemoz, G. English, D. Hui, K. Jenkins, P. Muench, G. Rao, G. Smith III, M. Sperling, K. Stawiasz, IBM TJ Watson Research Center, USA

SESSION 9 – HONOLULU SUITE
RF and New Wireless Transceivers

Thursday, June 17, 8:30 a.m.
Chairperson: C.M. Hung, Texas Instruments, Inc.
S. Mutoh, NTT Corp.

9.1 - 8:30 a.m.
A Quad-Band GSM/GPRS/EDGE SoC in 65nm CMOS, H. Darabi, P. Chang, H. Jensen, A. Zolfaghari, J. Leete, B. Mohammadi, J. Chiu, T. Li, X. Chen, Z. Zhou, M. Vadipour, C. Chen, Y. Chang, A. Mirzaei, A. Yazdi, M. Narima, A. Hadji, P. Lettieri, E. Chang, B. Zhao, K. Juan, P. Suri, C. Guan, L. Serrano, J. Leung, J. Shin, J. Kim, H. Tran, P. Kilcoyne, H. Vinh, E. Raith, M. Koscal, A. Hukkoo, C. Hayek, V. Rakhshani, C. Wilcoxson, M. Rofougaran, A. Rofougaran, Broadcom Corporation, USA

9.2 - 8:55 a.m.
A Carrier Leakage Auto-Calibration Circuit with a Direct DC-Offset Comparison Technique for a WiMAX Transmitter, H. Nakamoto, M. Kudo, H. Ito*, D. Yamazaki*, Fujitsu Microelectronics Ltd. Japan, *Fujitsu Laboratories Ltd

9.3 - 9:20 a.m.

1Gbps/ch 60GHz CMOS Multichannel Millimeter-Wave Repeater, A. Oncu, S. Ohashi*, K. Takano*, T. Takada**, J. Shimizu**, M. Fujishima, Hiroshima University, *The University of Tokyo, **Silicon Library Inc, Japan

9.4 - 9:45 a.m.
A 60-GHz FSK Transceiver with Automatically-Calibrated Demodulator in 90-nm CMOS, H. Wang, M.-H. Hung, Y.-C. Yeh, J. Lee, National Taiwan University, Taiwan

SESSION 10 – TAPA I
Advanced SRAM Circuits

Thursday, June 17, 10:25 a.m.
Chairperson: G. Lehmann, Infineon Technologies AG
T. Sekiguchi, Hitachi, Ltd.

10.1 - 10:25 a.m.
A 28-nm Dual-Port SRAM Macro with Active Bitline Equalizing Circuitry Against Write Disturb Issue, Y. Ishii, H. Fujiwara, K. Nii, H. Chigasaki, O. Kuromiya,T. Saiki, A. Miyanishi, Y. Kihara, Renesas Technology Corp, Japan

10.2 - 10:50 a.m.
Multi-Step Word-Line Control Technology in Hierarchical Cell Architecture for Scaled-Down High-Density SRAMs, K. Takeda, T. Saito, S. Asayama, Y. Aimoto, H. Kobatake, S. Ito, T. Takahashi, K. Takeuchi, M. Nomura, Y. Hayashi, NEC Electronics Corporation, Japan

10.3 - 11:15 a.m.
A Large σV_{TH}/VDD Tolerant Zigzag 8T SRAM with Area-Efficient Decoupled Differential Sensing and Fast Write-Back Scheme, J.-J. Wu, Y.H. Chen, M.-F. Chang, P.-W. Chou, C.-Y. Chen, H.-J. Liao, M.-B. Chen*, Y.-H. Chu*, W.-C. Wu*, H. Yamauchi**, National Tsing Hua University, Taiwan, *ITRI,Taiwan, **Fukuoka Institute of Technology, Japan

10.4 - 11:40 a.m.
A 32nm 8.3GHz 64-entry x 32b Variation Tolerant Near-Threshold Voltage Register File, A. Agarwal, S. Hsu, S. Mathew, M. Anders, H. Kaul, F. Sheikh, R. Krishnamurthy, Intel Corp, USA

SESSION 11 – HONOLULU SUITE
Advanced Clock Generation

Thursday, June 17, 10:25 am
Chairperson: J. Savoj, Qualcomm Inc.
C. Yoo, Hanyang University

11.1 - 10:25 a.m.
Generating Terahertz Signals in 65nm CMOS with Negative-Resistance Resonator Boosting and Selective Harmonic Suppression, Q.J. Gu, Z. Xu, H.-Y. Jian, X. Xu, M.-C.F. Chang, W. Liu, H. Fetterman, University of California, Los Angeles, USA

11.2 - 10:50 a.m.
An Over 20,000 Quality Factor On-Chip Relaxation Oscillator Using Power Averaging Feedback with a Chopped Amplifier, Y. Tokunaga, S. Sakiyama, S. Dosho, Panasonic Corporation, Japan

11.3 - 11:15 a.m.
A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology, B. Razavi, University of California, Los Angeles, USA

11.4 - 11:40 a.m.
A Frequency Accuracy Enhanced Sub-10µW On-Chip Clock Generator for Energy Efficient Crystal-Less Wireless Biotelemetry Applications, W.-H. Sung, S.-Y. Hsu, J.-Y. Yu, C.-Y. Yu, C.-Y. Lee, National Chiao Tung University, Taiwan

SESSION 12 – TAPA I
Digital Circuits Resilient

Thursday, June 17, 1:30 p.m.
Chairperson: V. De, Intel Corp.
M. Nomura, Renesas Electronics Corp.

12.1 - 1:30 p.m.
Resonant Supply Noise Canceller Utilizing Parasitic Capacitance of Sleep Blocks, J. Kim, T. Nakura, H. Takata*,K. Ishibashi*, M. Ikeda, K. Asada, University of Tokyo, Japan, *Renesas Technology Corporation, Japan

12.2 - 1:55 p.m.
On-Chip Waveform Capture and Diagnosis of Power Delivery in SoC Integration, T. Hashida, M. Nagata, Kobe University, Japan

12.3 - 2:20 p.m.
65nm Bistable Cross-coupled Dual Modular Redundancy Flip-Flop Capable of Protecting Soft Errors on the C-element, J. Furuta, C. Hamanaka*, K. Kobayashi*, H. Onodera, Kyoto University, Japan, Kyoto Institute of Technology, Japan

12.4 - 2:45 p.m.
Low-Cost Gate-Oxide Early-Life Failure Detection in Robust Systems, Y.M. Kim, Y. Kameda*, H. Kim, M. Mizuno*, S. Mitra, Stanford University, USA, *NEC Corporation, Japan

SESSION 13 – HONOLULU SUITE
RF Circuits and Systems

Thursday, June 17, 1:30 p.m.
Chairperson: B. Nauta, University of Twente
K. Agawa, Toshiba Corp.

13.1 - 1:30 p.m.
An On-Chip Wideband and Low-Loss Duplexer for 3G/4G CMOS Radios, M. Mikhemar, H. Darabi*, A. Abidi, University of California, Los Angeles, USA, *Broadcom Corporation, USA

13.2 - 1:55 p.m.
A 78 dB Dynamic Range, 0.27 dB Accuracy, Single-Stage RF-PGA using Thermometer-Weighted and Binary-Weighted Transconductors for SAW-less WCDMA/LTE Transmitters, M. Mizokami, Y. Furuta, T. Maruyama, H. Sato, Renesas Technology Corp., Japan

13.3 - 2:20 p.m.
A Low Energy Injection-Locked FSK Transceiver with Frequency-to-Amplitude Conversion for Body Sensor Applications, J. Bae, H.-J. Yoo, KAIST, Korea

13.4 - 2:45 p.m.
A 250 mV, 352 µW Low-IF Quadrature GPS Receiver in 130nm CMOS, A. Heiberg, T. Brown*, K. Mayaram*, T. Fiez*, Azuray Technologies, USA, *Oregon State University, USA

SESSION 14 – TAPA I
PLL and CDR

Thursday, June 17, 3:25 p.m.
Chairperson: I. Fujimori, Broadcom Corp.
H.-J. Park, Pohang Univ of Science and Tech.

14.1 - 3:25 p.m.
A 2.2GHz Sub-Sampling PLL with 0.16ps$_{rms}$ Jitter and -125dBc/Hz In-Band Phase Noise at 700µW Loop-Components Power, X. Gao, E. Klumperink, G. Socci*, M. Bohsali*, B. Nauta, University of Twente, The Netherlands, *National Semiconductor, USA

14.2 - 3:50 p.m.
A Compact 6 GHz to 12 GHz Digital PLL with Coupled Dual-LC Tank DCO, A. Goel, A. Rylyakov*, H. Ainspan*, D. Friedman*, University of Southern California, USA, *IBM T.J. Watson Research Center, USA

14.3 - 4:15 p.m.
A 9.2-12GHz, 90nm Digital Fractional-N Synthesizer with Stochastic TDC Calibration and -35/-41dBc Integrated Phase Noise in the 5/2.5GHz Bands, A. Ravi, S. Pellerano, C. Ornelas, H. Lakdawala, T. Tetzlaff, O. Degani, M. Sajadieh, K. Soumyanath, Intel Corp

14.4 - 4:40 p.m.
A 1.3-degree I/Q Phase Error, 7.1 – 8.7-GHz LO Generator with Single-Stage Digital Tuning Polyphase Filter, H. Kodama, H. Ishikawa, N. Oshima, A. Tanaka, NEC Corporation, Japan

14.5 - 5:05 p.m.
All-Digital CDR for High-Density, High-Speed I/O, M. Loh, A. Emami-Neyestanak, California Institute of Technology, USA

SESSION 15 – HONOLULU SUITE
High-Resolution and High Speed Data Converters

Thursday, June 17, 3:25 p.m.
Chairperson: J. Gealow, MediaTek Wireless, Inc.
S. Dosho, Panasonic Corp.

15.1 - 3:25 p.m.
A 14b 200MS/s DAC with SFDR>78dBc, IM3<-83dBc and NSD<-163dBm/Hz across the whole Nyquist Band enabled by Dynamic-Mismatch Mapping, Y. Tang, J. Briaire*, K. Doris*, R. van Veldhoven*, P. van Beek, H. Hegt, A. van Roermund, Eindhoven University of Technology, The Netherlands, *NXP, The Netherlands

15.2 - 3:50 p.m.
A 2.8-to-8.5mW GSM/Bluetooth/UMTS/DVB-H/WLAN Fully Reconfigurable CTΔΣ with 200kHz to 20MHz BW for 4G Radios in 90nm Digital CMOS, Y. Ke, P. Gao, J. Craninckx*, G. Van der Plas*, G. Gielen, K.U. Leuven, Belgium, *IMEC, Belgium

15.3 - 4:15 p.m.
A 0.02mm² 65nm CMOS 30MHz BW All-Digital Differential VCO-Based ADC with 64dB SNDR, J. Daniels, W. Dehaene, M. Steyaert, Andreas Wiesbauer*, K.U. Leuven, Belgium, *Infineon Technologies, Austria

15.4 - 4:40 p.m.
A 12-GS/s 81-mW 5-Bit Time-Interleaved Flash ADC with Background Timing Skew Calibration, M. El-Chammas, B. Murmann, Stanford University, USA

15.5 - 5:05 p.m.
A CMOS 6-Bit 16-GS/s Time-Interleaved ADC with Digital Background Calibration, C.-C. Huang, C.-Y. Wang, J.-T. Wu, National Chiao Tung University, Taiwan

JOINT TECHNOLOGY/CIRCUITS RUMP SESSION
Tuesday, June 15
8:00 p.m – 10:00 p.m.

Organizers:

Circuits	**Technology**
M. Whately, Cypress Semi.	T-J King Liu, Univ of California
M. Yamaoka, Hitachi	S. Yamakawa, Sony Corp.

RJ1: The Next Decade of VLSI Technology and Circuits – Are We on the Same Road?
Tapa 1

Moderators: J. Dawson, MIT
K. Kuhn, Intel

The International Technology Roadmap for Semiconductors (ITRS) charts future technology requirements and potential pathways for the industry to sustain the historical pace of improvement in *transistor* performance and cost. These include the use of higher-permittivity gate dielectric materials, high-mobility semiconductor channel materials, and non-classical structures to improve transistor drive current and scalability, and they vary depending on the application (high performance *vs.* low operating power *vs.* low standby power). The issues of increasing MOSFET off-state leakage current and performance variations with transistor scaling are fundamental challenges which will require joint Technology-Circuits solutions, in order for the industry to sustain the historical pace of improvement in *circuit* performance and cost.

This panel discussion will aim to answer the following questions:

- What do we expect to see in the next 10 years in terms of new devices and technologies? (Technologists will provide an ITRS-based perspective for future transistor improvement.)
- Will these address the needs of the expected applications? (Circuit designers will describe driver applications and associated device requirements in terms of performance, power, cost, and design complexity.)

Panelists:

M. Brillouet, CEA LETI
T. Hiramoto, Univ of Tokyo
K. Imai, NECEL
K. Ishibashi, Renesas Electronics Corp.
M. Izzard, Texas Instruments,
C. Phelan, Cypress Semi. Corp.
D. Robertson, Analog Devices,

CIRCUITS RUMP SESSION
Thursday, June 17
8:00 p.m – 10:00 p.m.

Organizers: J. Barth, IBM
M. Yamaoka, Hitachi

R1: A Role for VLSI in Green Technology?
Honolulu I

Organizers: J. Rabaey, University of California, Berkeley
M. Nomura, Renesas Electronics Corp.

Moderator: J. Rabaey, University of California, Berkeley

Green technology is all the rage (as is quite obvious from the investment community). One way to reduce our overall carbon footprint is to rethink in a profound way how we produce, transport, store and consume energy in a profound way. Information technology (supported by advanced networks of semiconductor devices) may have to play a major role in that process. In this panel, we explore a number of visions from different business segments of how this may transpire, what is needed to really make it happen, and what the roadblocks may be.

Panelists:
D. Freeman, Texas Instruments
M. Kondo, AIST
C. Lampe-Onnerud, Boston- Power
Y. Nishibe, Toyota

R2: Mixed Signal IP – Make vs. Buy
Honolulu II
Organizers: S. Nataragan, TSMC
K. Kajigaya, Elpida

Moderator: P. Rickert, Texas Instruments

With the increasing use of foundries across the industry, the question of when to make IP vs. when to buy IP is becoming more important. This panel is focused on the chip manufacturer's choice of design vs buy for complex mixed-signal IP. Panelists will represent larger chip vendors, fab-less IP providers and mixed signal IP consumers.

Panelists:

K. Arimoto, Renesas Electronics
J. Boufarhat, AMD
S-T Juang, TSMC
M. Keating, Synopsis
C. Mater, Qualcomm
S. Segars, ARM

SESSION 16 – TAPA I
Digital Processors

Friday, June 18, 8:30 a.m.
Chairperson: J. Farrell, Advanced Micro Devices
H. Kabuo, Panasonic Corp.

16.1 - 8:30 a.m.
Fine Grained Power Analysis and Low-Power Techniques of a 128GFLOPS/58W SPARC64™ VIIIfx Processor for Peta-scale Computing, H. Okano, Y. Kawabe*, R. Kan, T. Yoshida, I. Yamazaki, H. Sakurai, M. Hondou, N. Matsui, H. Yamashita, T. Nakada, T. Maruyama, T. Asakawa, Fujitsu Limited, *Fujitsu Laboratories Limited, Japan

16.2 - 8:55 a.m.
53Gbps Native GF$(2^4)^2$ Composite-Field AES-Encrypt/Decrypt Accelerator for Content-Protection in 45nm High-Performance Microprocessors, S. Mathew, F. Sheikh, A. Agarwal, M. Kounavis, S. Hsu, H. Kaul, M. Anders, R. Krishnamurthy, Intel Corporation, USA

16.3 - 9:20 a.m.
A 530Mpixels/s 4096x2160@60fps H.264/AVC High Profile Video Decoder Chip, D. Zhou, J. Zhou, X. He, J. Kong*, J. Zhu*, P. Liu*, S. Goto, Waseda University, Japan, *Shanghai Jiao Tong University, Japan

16.4 - 9:45 a.m.
Power Reduction Schemes in Next Generation Intel® ATOM™ Processor Based SoC for Handheld Applications., R. Islam, A. Sabbavarapu, R. Patel, Intel Corporation, USA

SESSION 17 – TAPA II
Interference Robust RF Receivers

Friday, June 18, 8:30 a.m.
Chairperson: L. Breems, NXP Semiconductors
H. Ishikuro, Keio University

17.1 - 8:30 a.m.
Quadrature Sampling Mixer Topology for SAW-Less GPS Receivers in 0.18µm CMOS, O. Ikeuchi, N. Saito, B. Nauta*, Asahi Kasei Microdevices Corporation, Japan, *University of Twente, The Netherlands

17.2 - 8:55 a.m.
A 65nm CMOS Quad-Band SAW-Less Receiver for GSM/GPRS/EDGE, A. Mirzaei, A. Yazdi, Z. Zhou, E. Chang, P. Suri, H. Darabi, Broadcom Corporation, USA

17.3 - 9:20 a.m.
A 6-phase Harmonic Rejection Down-Converter with Digital Assist, T. Yamaji, J. Matsuno, H. Aoyama, M. Furuta, T. Takida, I. Akita, A. Kuroda, T. Itakura, N. Itoh, Toshiba Corp, Japan

17.4 - 9:45 a.m.
0.6V, 5dB NF, -9.8dBm IIP_3, 900MHz Receiver with Interference Cancellation, A. Balankutty, P. Kinget, Columbia University, USA

SESSION 18 – TAPA I
DRAM

Friday, June 18, 10:25 a.m.
Chairperson: J. Barth, IBM Microelectronics
K. Kajigaya, Elpida Memory, Inc.

18.1 - 10:25 a.m.
1-Tbyte/s 1-Gbit DRAM Architecture with Micro-pipelined 16-DRAM Cores, 8-ns Cycle Array and 16-Gbit/s 3D Interconnect for High Throughput Computing, K. Ono, A. Kotabe, Y. Yanagawa, T. Sekiguchi, Hitachi, Ltd, Japan

18.2 - 10:50 a.m.
In-situ Measurement of Variability in 45-nm SOI Embedded DRAM Arrays, K. Agarwal, J. Hayes, J. Barth, M. Jacunski, K. Nowka, T. Kirihata, S. Iyer, IBM Corp, USA

18.3 - 11:15 a.m.
A 1.1V, 667MHz Random Cycle, Asymmetric 2T Gain Cell Embedded DRAM with a 99.9 Percentile Retention Time of 110µsec, K.C. Chun, P. Jain, T.-H. Kim, C. Kim, University of Minnesota, USA

18.4 - 11:40 a.m.
A 40nm 7Gb/s/pin Single-ended Transceiver with Jitter and HSI Reduction Techniques for High-Speed DRAM Interface, S.-J. Bae, Y.-S. Sohn, T.-Y. Oh, S.-H. Kwak, D.-M. Kim, D.-H. Kim, Y.-S. Kim, Y.-S. Yang, S.-Y. Doo, J.-I. Lee, S.-Y. Bang, S.-Y. Park, K.-W. Yeom, J.-Y. Lee, H. Park, W.-S. Kim, H.-J. Yang, K.-I. Park, J.S. Choi, Y.-H. Jun, Samsung Electronics, Korea

SESSION 19 – TAPA II
Digital Chip-to-Chip and On-Die Interfaces

Friday, June 18, 10:25 a.m.
Chairperson: A. Bhavnagarwala, IBM TJ Watson Research
R. Woo, LG Electronics

19.1 - 10:25 a.m.
A 2.5kV Isolation 35kV/us CMR 250Mbps 0.13mA/Mbps Digital Isolator in Standard CMOS with an On-Chip Small Transformer, S. Kaeriyama, S. Uchida*, M. Furumiya*, M. Okada*, M. Mizuno, NEC Corporation, Japan, *NEC Electronics Corp., Japan

19.2 - 10:50 a.m.
Simultaneous 6Gb/s Data and 10mW Power Transmission using Nested Clover Coils for Non-Contact Memory Card, Y. Yuan, A. Radecki, N. Miura, L.I. Aikawa, Y. Take, H. Ishikuro, T. Kuroda, Keio University, Japan

19.3 - 11:15 a.m.
A 0.7V 20fJ/bit Inductive-Coupling Data Link with Dual-Coil Transmission Scheme, N. Miura, T. Shidei, Y. Yuxiang, S. Kawai, K. Takatsu, Y. Kiyota, Y. Asano, T. Kuroda, Keio University, Japan

19.4 - 11:40 a.m.
2.4GHz 7mW All-Digital PVT-Variation Tolerant True Random Number Generator in 45nm CMOS, S. Srinivasan, S. Mathew, R. Ramanarayanan, F. Sheikh, M. Anders, H. Kaul, V. Erraguntla, R. Krishnamurthy, G. Taylor, Intel Corporation, USA

HONOLULU SUITE
2010 Circuits Luncheon
(Separate Registration Required)

Friday, June 18, 12:00 p.m.

Alan Blumlien – The Greatest Circuit Designer, Ever?
Asad Abidi, Electrical Engineering, University of California, Los Angeles

We know by name many of the people who invented widely used circuits in the microelectronics era. They were the ones who showed us how to design robust circuits with an awareness of the unique aspects of a monolithic substrate. But many of the circuit topologies they used hark back to vacuum-tube discrete circuits, yet the inventors of those circuit shapes---the giants on whose shoulders our monolithic pioneers stood---remain relatively obscure.
In this lunchtime talk, I will make the case for one such giant, whose sheer number of circuit inventions that remain in use today make him, in my mind, the most likely candidate for the greatest circuit designer, ever.

SESSION 20 – TAPA I
Signal Processing for Wireless

Friday, June 18, 1:45 p.m.
Chairperson: B. Nikolic, University of California, Berkeley
M. Hariyama, Tohoku University

20.1 - 1:45 p.m.
A 1-190MSample/s 8-64 Tap Energy-Efficient Reconfigurable FIR Filter for Multi-Mode Wireless Communication, F. Sheikh, M. Miller, B. Richards, D. Markovic, B. Nikolic, University of California, Berkeley, USA

20.2 - 2:10 p.m.
A 5.8mW 3GPP-LTE Compliant 8x8 MIMO Sphere Decoder Chip with Soft-Outputs, C.-H. Yang, T.-H. Yu, D. Markovic, University of California, Los Angeles, USA

20.3 - 2:35 p.m.
A 4.84 mm^2 847-955 Mb/s 397 mW Dual-Path Fully-Overlapped QC-LDPC Decoder for the WiMAX System in 0.13 µm CMOS, B. Xiang, X. Zeng, Fudan University, China

20.4 - 3:00 p.m.
A 10.37 mm2 675 mW reconfigurable LDPC and Turbo encoder and decoder for 802.11n, 802.16e and 3GPP-LTE, F. Naessens, V. Derudder, H. Cappelle, L. Hollevoet, P. Raghavan, M. Desmet, A. AbdelHamid, I. Vos, L. Folens, S. O'Loughlin, S. Singirikonda, S. Dupont, J.-W. Weijers, A. Dejonghe, L. Van der Perre, IMEC, Belgium

SESSION 21 – TAPA II
Biosensors

Friday, June 18, 1:45 p.m.
Chairperson: J. Dawson, MIT
M. Ikeda, University of Tokyo

21.1 - 1:45 p.m.
A Digitally-Assisted Sensor Interface for Biomedical Applications, J.L. Bohorquez, M. Yip, A.P. Chandrakasan, J.L. Dawson, Massachusetts Institute of Technology, USA

21.2 - 2:10 p.m.
A 2.4µA Continuous-time Electrode-Skin Impedance Measurement Circuit For Motion Artifact Monitoring in ECG Acquisition Systems, S. Kim, R.F. Yazicioglu, T. Torfs, B. Dilpreet, P. Julien, C. Van Hoof, IMEC, Belgium

21.3 - 2:35 p.m.
A Low Power CMOS Receiver for a Tissue Monitoring NMR Spectrometer, J. Kim, B. Hammer, R. Harjani, University of Minnesota, USA

21.4 - 3:00 p.m.
An Activity-Dependent Brain Microstimulation SoC with Integrated 23nV/rtHz Neural Recording Front-End and 750nW Spike Discrimination Processor, M. Azin, D. Guggenmos*, S. Barbay*, R. Nudo*, P. Mohseni, Case Western Reserve University, *Kansas University Medical Center, USA

SESSION 22 – TAPA I
Nonvolatile Memories

Friday, June 18, 3:40 p.m.
Chairperson: O. Jungroth, Intel Corporation
N. Lu, Etron Technology, Inc.

22.1 - 3:40 p.m.
A 100MHz Ladder FeRAM Design with Capacitance-Coupled-Bitline (CCB) Cell, D. Takashima, Y. Nagadomi, T. Ozaki, Toshiba Corp, Japan

22.2 - 4:05 p.m.
A Low Store Energy, Low VDDmin, Nonvolatile 8T2R SRAM with 3D Stacked RRAM Devices for Low Power Mobile Applications, P.-F.Chiu, M.-F. Chang, S.-S. Sheu*, *K.-F. Lin, P.-C. Chiang*, C.-W. Wu, W.-P. Lin*, C.-H. Lin*, C.-C. Hsu, F.T. Chen*, K.-L. Su*, M.-J. Kao*, M.-J. Tsai*, National Tsing Hua University, Taiwan, *EOL, ITRI, Taiwan

22.3 - 4:30 p.m.
OxID: On-Chip One-Time Random ID Generation Using Oxide Breakdown, N. Liu, S. Hanson, D. Sylvester, D. Blaauw, University of Michigan, USA

22.4 - 4:55 p.m.
A 60% Higher Write Speed, 4.2Gbps, 24-Channel 3D-Solid State Drive (SSD) with NAND Flash Channel Number Detector and Intelligent Program-Voltage Booster, T. Hatanaka, K. Ishida, T. Yasufuku, S. Miyamoto*, H. Nakai*, M. Takamiya, T. Sakurai, K. Takeuchi, University of Tokyo, *Toshiba Corporation, Japan

SESSION 23 – TAPA II
Low-Power Nyquist ADCs

Friday, June 18, 3:40 p.m.
Chairperson: U. Moon, Oregon State University
M. Yoshioka, Fujitsu Laboratories Ltd.

23.1 - 3:40 p.m.
A Zero-Crossing Based 12b 100MS/s Pipelined ADC with Decision Boundary Gap Estimation Calibration, J. Chu, L. Brooks*, H.-S. Lee, Massachusetts Institute of Technology, *Ubixum, Inc., USA

23.2 - 4:05 p.m.
A 12b 50MS/s 3.5mW SAR Assisted 2-Stage Pipeline ADC, C. Lee, M. Flynn, University of Michigan, USA

23.3 - 4:30 p.m.
A 1V 11fJ/Conversion-Step 10bit 10MS/s Asynchronous SAR ADC in 0.18µm CMOS, C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, C.-M. Huang*, National Cheng Kung University, Taiwan, *Himax Technologies, Inc., Taiwan

23.4 - 4:55 p.m.
A 9-bit 150-MS/s 1.53-mW Subranged SAR ADC in 90-nm CMOS, Y.-Z. Lin, C.-C. Liu, G.-Y. Huang, Y.-T. Shyu, S.-J. Chang, National Cheng Kung University, Taiwan

GENERAL INFORMATION

SCOPE OF SYMPOSIUM
The scope of the Symposium covers all aspects of VLSI circuits, such as Circuit design to address challenges of deeply scaled technologies - e.g. DFM, variability, reliability; digital circuit techniques; analog and mixed signal circuits such as data converters and amplifiers to address performance, power, technology scaling, and variability; complex SOC systems describing new architectures and implementations; circuit approaches for clock generation and distribution; advances in memory circuits; especially for embedded memories in scaled technologies; power minimization techniques for analog and digital circuits, including novel energy harvesting, battery management and renewable energy topics; power management circuits, including linear and switching voltage regulators and voltage references.
- Techniques for digitally-assisted analog and analog-assisted digital including digital implementation of previously analog functions; architectures and circuits for RF and wireless communications; circuits for sensors and displays; wireline transceiver and I/O design optimized for high bandwidth and low-power spanning from chip-to-chip through long-reach applications; fundamentals related to the above, including innovative transistor-level circuit design and circuits for characterizing technology changes and variations.

REGISTRATION INFORMATION:
When you register on-site, an additional $75 will be added to the registration fees.

Payment of the registration fee entitles the registrant to one copy of the Technical Digest, one CD-ROM, one banquet and one reception ticket.

	Member	NonMember	Students
Tech Short Course	$295	$395	$100
Tech Symposium	$550	$650	$275
Circ Short Course	$350	$450	$125
Circ Symposium	$550	$650	$275
Circuits Luncheon	$50	$50	$50
Digest	$75	$75	$75
Add'l Short Course books	$95	$95	$95
Banquet Tickets	$85	$85	$85

REGISTRATION: Credit Cards (MasterCard/Visa/Amex), personal checks, company checks or traveler's checks payable to the 2010 VLSI Symposia **in U.S. Dollars** are the only acceptable forms of payment. All checks must be drawn on U.S. banks.

CANCELLATION POLICY: All requests for refunds for registrations paid in US dollars must be made in writing and submitted by June 1, 2010 to VLSI c/o Yes Events, PO Box 32862, Baltimore, MD 21282, USA
Telephone: US Reg: 1-800-937-8728, Int'l Reg: +1-410-559-2236
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There will be a fee of $30 for all cancellations. No refunds will be issued for cancellations received after June 1. 2010. All refunds will be processed after the Symposia.

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	Single/Double
Garden View	$219.00
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Deluxe Ocean View	$265.00
Alii Ocean View	$295.00

All rooms are subject to an 11.96% combined tax. To make a room reservation, go to www.vlsisymposium.org, click the tab at the top of the screen labeled Travel/Reservation Information. Click on the link for the hotel reservations.

All reservations must be accompanied by advanced deposit or guaranteed by a credit card in order to guarantee the reservation. A confirmation will be mailed to you directly by the hotel. Check-in time is 2:00 pm and check-out is 11:00 am.

The hotel offers both non-smoking and handicapped rooms. Please make these specific requests when you make your hotel reservation.

TRANSPORTATION FROM THE HONOLULU INTERNATIONAL AIRPORT TO THE HILTON HAWAIIAN VILLAGE: Airport Express Shuttle and taxi services are available from the Honolulu International Airport to the hotel and return. Shuttle fare is approximately $15.00 each way. From the hotel to the airport you need to make a reservation one day in advance. Taxi fare is approximately $30.00 one way.

VISA REQUIREMENTS FOR ENTRY INTO U.S.: Citizens of foreign countries must have in their possession a valid passport and visa upon entering the United States. Foreign participants should contact the United States Embassy, Consulate, or Office of Tourism in their home country AS SOON AS POSSIBLE to determine their particular visa requirements.

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Sunday, June 13	4:00 pm – 6:00 pm
Monday, June 14	7:30 am - 5:00 pm
Tuesday, June 15	7:30 am - 5:00 pm
Wednesday, June 16	7:30 am - 5:00 pm
Thursday, June 17	8:00 am – 5:00 pm
Friday, June 18	8:00 am – 3:00 pm

SYMPOSIA ON VLSI TECHNOLOGY AND VLSI CIRCUITS RECEPTION: A joint reception for both Technology and Circuits will be held on Tuesday, June 15 from 6:00 pm to 8:00 pm on the Lagoon Green.

SYMPOSIA ON VLSI TECHNOLOGY AND VLSI CIRCUITS BANQUET: The 2010 Symposia on VLSI Technology and VLSI Circuits Banquet will be held on Wednesday, June 17 on the Lagoon Green from 7:00 pm to 9:00 pm. Banquet tickets for accompanying guests can be purchased at the Registration desk in the Palace Lounge Lobby.

SPEAKER PREPARATION CENTER: There will be a designated Speaker Preparation Room. Specifics will be available at the Registration Desk located in the Palace Lounge Lobby.

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