

Design Methodology and Tools in an evolving CMOS Technology (NAE)

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New and evolving CMOS technologies already covered in this course present many special challenges for digital and mixed analog SOC designers. This section of the short course will discuss these critical DSM issues in the context of large SOC designs. It will cover a range of methodologies and design techniques available to digital designers to model, bound, correct and in some cases avoid these DSM effects. Several recent design examples will also be used to illustrate some of these approaches. These effects all have to be comprehended in an efficient manner to allow competitive design time, power, performance, area and yields. We will discuss several DSM effects such as CMP, xBTI, leakage power, Local miss-match, Global variance, litho, stress context and others. These are relevant issues for all digital designers. However the large SOC chip designer often has to use different techniques and tools from the transistor level designer. There are several driving factors, but problem size alone for modern 100M+ gate designs often dictates different approaches to the problem.