SESSION 11 – HONOLULU SUITE
Advanced Clock Generation

Thursday, June 17, 10:25 am
Chairperson: J. Savoj, Qualcomm Inc.
C. Yoo, Hanyang University

11.1 - 10:25 a.m.
Generating Terahertz Signals in 65nm CMOS with Negative-Resistance Resonator Boosting and Selective Harmonic Suppression, Q.J. Gu, Z. Xu, H.-Y. Jian, X. Xu, M.-C.F. Chang, W. Liu, H. Fetterman, University of California, Los Angeles, USA

Terahertz signals have been successfully generated in 65nm CMOS by: 1) stacking a negative-resistance resonator in parallel to the conventional resonant tank to boost the fundamental oscillation frequency; and by 2) selectively suppressing the odd and 2nd harmonics to boost the 4th and 6th harmonics in the terahertz regime. Consequently, we have detected 4th and 6th harmonic signals through on-chip antenna radiation at 0.87 and 1.31 THz, respectively.

11.2 - 10:50 a.m.
An Over 20,000 Quality Factor On-Chip Relaxation Oscillator using Power Averaging Feedback with a Chopped Amplifier, Y. Tokunaga, S. Sakiyama, S. Dosho, Panasonic Corporation, Japan

This paper describes the first achievement of over 20,000 quality factors among on-chip relaxation oscillators. The proposed Power Averaging Feedback with a Chopped Amplifier enables such a high Q which is close to MEMS oscillators. 1/f noise free design and rail-to-rail oscillation result in low phase noise with small area and low power consumption. The proposed oscillator can be applied to low noise applications (e.g. digital audio players) implemented onto a System on a Chip.

11.3 - 11:15 a.m.
A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology, B. Razavi, University of California, Los Angeles, USA

Magnetic feedback from a differential pair to the core of a cross-coupled oscillator reduces the effect of device losses, raising the oscillation frequency. Three prototypes using one-turn nested inductors and including on-chip downconversion mixers operate at 205 GHz, 240 GHz, and 300 GHz while drawing a power of 3.5 mW.

11.4 - 11:40 a.m.
A Frequency Accuracy Enhanced Sub-10μW On-Chip Clock Generator for Energy Efficient Crystal-Less Wireless Biotelemetry Applications, W.-H. Sung, S.-Y. Hsu, J.-Y. Yu, C.-Y. Yu, C.-Y. Lee, National Chiao Tung University, Taiwan

A frequency accuracy enhanced clock generator is proposed for energy efficient crystal-less WBAN system. By applying a self-reference calibration and tracking a remote downlink wireless reference, the robust system clock with ±30ppm accuracy against both 20% voltage variation and 75°C temperature variation is developed to enable over-Mbps uplink data transmission. Furthermore, the clock generator based on hysteresis delay cells consumes 7.6μW in 5MHz and is able to minimize significant always-on clock source power.