SESSION 13 – HONOLULU SUITE
**RF Circuits and Systems**

Thursday, June 17, 1:30 p.m.
Chairperson: B. Nauta, University of Twente
K. Agawa, Toshiba Corp.

**13.1 - 1:30 p.m.**
**An On-Chip Wideband and Low-Loss Duplexer for 3G/4G CMOS Radios,** M. Mikhemar, H. Darabi*, A. Abidi, University of California, Los Angeles, USA, *Broadcom Corporation, USA

A wideband integrated RF duplexer supports 3G/4G bands I, II, III, IV, and IX, and achieves a TX-to-RX isolation of more than 55dB in the transmit-band, and greater than 45dB in the corresponding receive-band across 200MHz of bandwidth. A 65nm CMOS duplexer/LNA achieves a transmit insertion loss of 2.5dB, and a cascaded receiver noise figure of 5dB with more than 27dB of gain, exceeding the commercial external duplexers performance at considerably lower cost and area.

**13.2 - 1:55 p.m.**
**A 78 dB Dynamic Range, 0.27 dB Accuracy, Single-Stage RF-PGA using Thermometer-Weighted and Binary-Weighted Transconductors for SAW-less WCDMA/LTE Transmitters,** M. Mizokami, Y. Furuta, T. Maruyama, H. Sato, Renesas Technology Corp., Japan

A single-stage RF programmable gain amplifier (RF-PGA) in 65-nm CMOS is presented. The RF-PGA consists of thermometer-weighted transconductors and binary-weighted transconductors with an R-2R ladder. The transmitter prototype with the single-stage RF-PGA achieves 78 dB dynamic range, 0.27 dB accuracy in 1dB step at 1950 MHz. The measured transmitter noise in RX band is -160.4 dBc/Hz. The ACLR and EVM with LTE modulated signal (BW=20 MHz) are -40 dBc and 3.4 %, respectively.

**13.3 - 2:20 p.m.**
**A Low Energy Injection-Locked FSK Transceiver with Frequency-to-Amplitude Conversion for Body Sensor Applications,** J. Bae, H.-J. Yoo, KAIST, Korea

A novel injection-locked frequency divider (ILFD) based transceiver with one-to-one frequency-to-amplitude conversion is proposed and implemented for body sensor applications. The efficient FSK direct modulation transmitter and envelope detection receiver enables ultra low energy data transmission. As a result, the transceiver achieves the most energy-efficient performance compared with state-of-the-art works.

**13.4 - 2:45 p.m.**
**A 250 mV, 352 µW Low-IF Quadrature GPS Receiver in 130nm CMOS,** A. Heiberg, T. Brown*, K. Mayaram*, T. Fiez*, Azuray Technologies, USA, *Oregon State University, USA

A low-IF quadrature GPS receiver consisting of a VCO, mixer and variable gain LNA is implemented in 130 nm CMOS. Consuming 352 µW from a 250 mV supply, it has the lowest supply voltage for an integrated receiver reported to date. The measured noise figure is 7.2 dB with a gain of 42 dB at a 10 MHz IF frequency. At a 1 MHz offset, the VCO phase noise is -112.4 dBc/Hz, resulting in an FoM of 187.4 dBc/Hz.