SESSION 14 – TAPA I
PLL and CDR

Thursday, June 17, 3:25 p.m.
Chairperson: I. Fujimori, Broadcom Corp.
H.-J. Park, Pohang University of Science and Technology

14.1 - 3:25 p.m.
A 2.2GHz Sub-Sampling PLL with 0.16ps$_{rms}$ Jitter and -125dBc/Hz In-Band Phase Noise at 700µW Loop-Components Power, X. Gao, E. Klumperink, G. Socci*, M. Bohsali*, B. Nauta, University of Twente, The Netherlands, *National Semiconductor, USA

A divider-less PLL exploits a phase detector that directly samples the VCO with a reference clock. No VCO sampling buffer is used while dummy samplers keep the VCO spur <-56dBc. A modified inverter with low short-circuit current acts as a power efficient reference clock buffer. The 2.2GHz PLL in 0.18µm CMOS achieves -125dBc/Hz in-band phase noise with only 700µW loop-components power.

14.2 - 3:50 p.m.
A Compact 6 GHz to 12 GHz Digital PLL with Coupled Dual-LC Tank DCO, A. Goel, A. Rylyakov*, H. Ainspan*, D. Friedman*, University of Southern California, USA, *IBM T.J. Watson Research Center, USA

A digital PLL, realized in 45nm SOI CMOS, features a dual LC-tank DCO with nested inductors, achieving an octave of tuning range and area of 0.111 mm^2. Digital control of coupled LC-tanks creates new capabilities, enabling a 10% increase in tuning range and a 28 times reduction of DCO gain. The rms jitter, integrated from fc/1667 to fc/2, is 362 fs at 12 GHz and 274 fs at 6 GHz.

14.3 - 4:15 p.m.
A 9.2-12GHz, 90nm Digital Fractional-N Synthesizer with Stochastic TDC Calibration and -35/-41dBc Integrated Phase Noise in the 5/2.5GHz Bands, A. Ravi, S. Pellerano, C. Ornelas, H. Lakdawala, T. Tetzlaff, O. Degani, M. Sajadieh, K. Soumyanath, Intel Corp

A 90nm CMOS, 9.2-12GHz digital fractional-N synthesizer for WLAN/WiMax is described. Stochastic calibration of time to digital conversion and VCO phase noise minimization algorithms are used to achieve <-35dBc integrated phase nose (100Hz to 10MHz), in the 5-6GHz band with spurs below -60dBc.

14.4 - 4:40 p.m.
A 1.3-degree I/Q Phase Error, 7.1 – 8.7-GHz LO Generator with Single-Stage Digital Tuning Polyphase Filter, H. Kodama, H. Ishikawa, N. Oshima, A. Tanaka, NEC Corporation, Japan

We have developed an LO generator having 1) a digitally I/Q imbalance tuning polyphase filter and 2) a PLL with a varactor-based VCO and an interleaved charge pump for wide frequency operation. A 90-nm CMOS implementation showed that the equivalent maximum phase error was below 1.3 degrees in 7.1 – 8.7-GHz frequency range.

14.5 - 5:05 p.m.
All-Digital CDR for High-Density, High-Speed I/O, M. Loh, A. Emami-Neyestanak, California Institute of Technology, USA

A novel all-digital CDR for source-synchronous links, and its implementation in 90nm CMOS, is presented. A phase alignment technique with ping-pong action between two clock phases is used. The system is implemented in static CMOS logic, occupies 0.234 mm^2 and dissipates 16.6 mW at 6 Gb/s, demonstrating BER < 10^{-13} with PRBS-7 input. The compactness and all-static-CMOS nature of the system make it suitable for use in high-speed I/Os requiring per-pin synchronization.