SESSION 4 – TAPA I
SRAM Variability

Wednesday, June 16, 1:30 p.m.
Chairperson: M. Whately, Cypress Semiconductor
H. Yamauchi, Fukuoka Institute of Technology

4.1 - 1:30 p.m.
Dynamic SRAM Stability Characterization in 45nm CMOS, S.O. Toh, Z. Guo, B. Nikolic, University of California, Berkeley, USA

A method for characterizing dynamic SRAM stability using pulsed wordlines, is demonstrated in 45nm CMOS. Static read margins were observed to overestimate failures by up to 1000x while static write margins failed to predict outliers in dynamic write stability. Dynamic write stability was demonstrated to exhibit an enhanced sensitivity to process variations, and negative bias temperature instability (NBTI), compared to static write margins.

4.2 - 1:55 p.m.
Small-Defect Detection in sub-100nm SRAM Cells using WL-Pulse Timing-Margin Measurement Scheme, Y. Morita, K. Nose, K. Noguchi, S. Takami*, K. Goto*, S. Aimoto*, A. Kimura*, M. Mizuno, NEC Corporation, Japan, *NEC Electronics Corporataion, Japan

The detection of small defects in an SRAM cell with our WL-pulse timing-margin measurement scheme has been demonstrated on a 90nm 2Mb SRAM. WL-width control with a high resolution of 24.1ps and a wide range improves the sensitivity of detection for delay and SNM variations with only a 0.6% area overhead, and statistical analysis makes possible the detection of small-delay defects that, in conventional testing, would be buried due to delay variations in peripheral circuitry.

4.3 - 2:20 p.m.
Tunable Replica Bits for Dynamic Variation Tolerance in 8T SRAM, A. Raychowdhury, B. Gueskens, K. Bowman, J. Tschanz, S.-L. Lu, T. Karnik, M. Khellah, V. De, Intel Corp, USA

Infrequent dynamic events like VCC droops and temperature changes result in the use of a static VCC guard-band in memory arrays. Measured data on a 16KB 8T array featuring tunable replica bits illustrate the opportunity of eliminating a majority of the static guard-band resulting in lower operating VCC/power.

4.4 - 2:45 p.m.
70% Read Margin Enhancement by V_{TH} Mismatch Self-Repair in 6T-SRAM with Asymmetric Pass Gate Transistor by Zero Additional Cost, Post-Process, Local Electron Injection, K. Miyaji, S. Tanakamaru, K. Honda, S. Miyano*, K. Takeuchi, University of Tokyo, Japan, *Semiconductor Technology Academic Research Center (STARC), Japan

Read margin of the 6T-SRAM cell is enhanced by 70% with the proposed V_{TH} mismatch self-repair scheme utilizing asymmetric pass gate transistor. The asymmetric V_{TH} transistor is realized by local electron injection after process. Measurements show twice as large asymmetric V_{TH} shift from the past work without process and area penalty. 24% static noise margin increase is experimentally demonstrated with the proposed asymmetric pass gate transistor without degradation in write characteristics.