SESSION 8 – TAPA I

**High Speed On-Die Network and Processor Clocking**

Thursday, June 17, 8:30 a.m.
Chairperson: S. Tam, Intel Corporation
K. Nose, Renesas Corporation

**8.1 - 8:30 a.m.**

**A 2Tb/s 6×4 Mesh Network with DVFS and 2.3Tb/s/W router in 45nm CMOS,** P. Salihundam, S. Jain, T. Jacob, S. Kumar, V. Erraguntla, Y. Hoskote, S. Vangal, G. Ruhl, P. Kundu, N. Borkar, Intel Corporation

A packet-switched 6x4 2D mesh network-on-chip (NoC) on a dedicated voltage and frequency island (VFI) provides 2Tb/s of bisection bandwidth, and interconnects 48 PentiumTM class IA-32 cores and 4 DDR3 channels. The 1.28Tb/s router with 16B, 5.4mm links achieves high network utilization through 8 virtual channels (VC), early-buffer write and read, route pre-computation and a 1-cycle wrapped wavefront allocator (WWFA) design. The 640K transistor, 1.17mm$^2$ router operates at 2GHz at 1.1V while dissipating 550mW. Router energy efficiency scales up to 7.2Tb/s/W.

**8.2 - 8:55 a.m.**

**A 1.07 Tbit/s 128×128 Swizzle Network for SIMD Processors,** S. Satpathy, Z. Foo, B. Giridhar, D. Sylvester, T. Mudge, D. Blaauw, University of Michigan, USA

A novel circuit switched swizzle network called XRAM is presented. XRAM uses an SRAM-based approach producing a compact footprint that scales well with network dimensions while supporting all permutations and multicasts. Capable of storing multiple shuffle configurations and aided by a novel sense-amp for robust bit-line evaluation, a 128×128 XRAM fabricated in 65nm achieves a bandwidth exceeding 1Tbit/s, enabling a 64-lane SIMD engine operating at 0.72V to save 46.8% energy over an iso-throughput conventional 16-lane implementation at 1.1V.

**8.3 - 9:20 a.m.**

**A Scalable, Sub-1W, Sub-10ps Clock Skew, Global Clock Distribution Architecture for Intel® Core™ i7/i5/i3 Microprocessors,** G. Shamanna, N. Kurd, J. Douglas, M. Morrise, Intel Corporation, USA

This paper describes global clock distribution architecture of Intel® Core™ i7/i5/i3 microprocessor family. Highlight of this paper is a pseudo-recombinant clock distribution architecture successfully implemented in 32nm/45nm generation of CoreTM i7/i5/i3 processors. This clock distribution topology achieves less than 10ps clock skew while consuming a maximum power of 1 Watt across entire operating voltage and frequency range.

**8.4 - 9:45 a.m.**

**A DPLL-based per Core Variable Frequency Clock Generator for an Eight-Core POWER7™ Microprocessor,** J. Tierno, A. Rylyakov, D. Friedman, A. Chen, A. Ciesla, T. Diemoz, G. English, D. Hui, K. Jenkins, P. Muench, G. Rao, G. Smith III, M. Sperling, K. Stawiasz, IBM TJ Watson Research Center, USA

A per-core clock generator for the eight-core POWER7™ processor is implemented with a digital PLL. This frequency generator is capable of smooth, controlled frequency slewing, minimizing the impact of di/dt. Frequency can be dynamically adjusted while the clock is running and processor instructions are executing, and without skipping any cycles, thus enabling aggressive power management techniques.