

CMOS Technology Trends

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As CMOS technology generations have been moving beyond 90 nm, there have been significant changes in features at every node: They include introduction of high K, increase in leakage, more structured lay-out, and the drop in supply voltage (at slower pace than predicted by scaling theory), the metallization trends (in particular the electromigration trends), and the introduction of 3D. In this talk we will look at the key technology features starting at 90 nm and up to 15 nm, and discuss how they impact the designs (both in high performance and low-power space). We will look at supply voltage trends and its impact on power density and SRAM functionality. Device leakage and variability have been going up, and the minimum device leakage will continue to increase. This will be an increasing challenge, particularly in the low power space. In this context, we will talk about fully-depleted devices and how they may help the leakage and variability. We will review the back bias techniques and the increasing challenges there from the diminishing body effect (and possible technology solutions). We will talk about the BEOL trends (reliability and performance) and the increasing challenges as the BEOL pitch moves below 100 nm. Finally we will touch on the density challenge: at 15-11 nm nodes, where the device count will be >1 billion /cm². Chips with that many devices will pose tremendous challenges in design, verification, and in the application space.