Clocking techniques for high-speed wireline,
by Jae-Yoon Sim, POSTECH Korea

The trend of multi-functionality and high-definition imaging has driven rapid increase in the amount of data communicating through wireline links and achieved the data rate of above 10 Gb/s/pin with scaled CMOS technologies. This talk reviews various architectures and circuits of clocking schemes used in high-speed and low-power serial/parallel links. Clock recovery circuits and source synchronous clocking schemes will be covered in detail.