## 6. Memory Design

### (i) Low Power DRAM Circuit & Interface Design

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As higher data rate up to 10 Gbps is demanded not only in graphics DRAM but also in main-memory DRAM for PCs and servers, the power consumption has become much more critical. As DRAM has become a key component in consumer electronics and mobile appliances, the standby power is also in focus. In this short course, low-power, high-speed DRAM interface and its circuits employed such as fast recovery DLL and PLL will be extensively reviewed for DRAM users and circuit designers. Next, low-voltage, high-performance DRAM peripheral circuits such as low-leakage sense amplifier will be introduced. Then, system-level low-power solutions such as asymmetric memory interface will be discussed. Finally, future direction including 3D chip stack will be presented.

### (ii) Disturbance and interference issues in NAND Flash design

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Aggressive scaling and introduction of MLC has made NAND Flash memory highly low-cost and thus successful in the high capacity multi-media applications market. Among the issues regarding technology scaling, the program disturbance and interference between cells have been the major issues affecting the yield and reliability. Until early 2000s, these issues were managed by the optimization of manufacturing process. But, with the introduction of MLC to NAND Flash memory, the reduced sensing margin has reached the level that simple process optimizations can not remedy the program disturbance and interference issues. Therefore, various design techniques have been developed and employed to guarantee the yield and reliability for each technology generation in addition to the process optimization efforts. In this short course, the program disturbance and interference issues will be summarized first, and then various countermeasures in each technology generation will be reviewed. Lastly, the future direction for NAND Flash memory design will be presented.