2010 Symposium on VLSI Circuits

Honolulu, June 15-18
Pre-Conference Publicity
www.vlsisymposium.org
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Agenda

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2010 Symposia on VLSI Circuits and Technology in Honolulu, Hawaii on 15-18 June

Continuing the trend of the last two years, the 24th annual VLSI Circuits Symposium will overlap the VLSI Technology Symposium by two full days to allow attendees to attend papers from both. The Circuits conference, sponsored by the Solid-State Circuits Society, will be on 16-18 June; the Technology conference will be on 15-17 June.

Circuits Symposium Technical Program will focus on "**Looking to the Next Decade of Electronics**" as we consider the changing landscape and challenges in the semiconductor industry over the coming years.

Calendar

Tuesday 6/15		Wednesday 6/16		Thursday 6/16		**Friday 6/18**	
Early AM	Hon 1 and 2	Tapa 2		Tapa 1	Honolulu	Tapa 1	Tapa 2
	Short courses	Plenary Session		High Speed On-Die Network and Processor Clocking	RF and New W Transceivers	Digital Processors	Interference Robust RF Receivers
Late AM	Hon 1 and 2	Tapa 1	Honolulu	Tapa	Honolulu	Tapa 1	Tapa 2
	Short courses	Medical and Vision Processors	UWB Circuits	SRAM Circuits	Advanced Clock Generation	DRAM	Digital Chip-to-Chip and On-Die Interfaces
Early PM	Hon 1 and 2	Tapa 1	Honolulu	Tapa 1	Honolulu	Tapa 1	Tapa 2
	Short courses	SRAM Variability	Clocking Building Blocks	Digital Circuits Resilent	RF Circuits and Systems	Signal Processing for Wireless	Biosensors
Late PM	Hon 1 and 2	Tapa 1	Honolulu	Tapa 1	Honolulu	Tapa 1	Tapa 2
	Short courses	Analog Circuits	Advanced Transceivers Techniques	PLL and CDR	High-Resolution and High Speed Data Converters	Nonvolatile Memories	Low-Power Nyquist ADCs
Evening	Joint Reception Tech Rumps	Joint Banquet		Circuit Rumps			

Key Speakers

- **Plenary Speaker: Dr. Christina Lampe-Onnerud of Boston Power** on "Opportunities in Energy Storage due to the Paradigm Shift Fueled by the Mobile and Clean Tech Revolutions"
- **Plenary Speaker: Dr. Satoru Fujikawa of Panasonic** on "Three-Dimensional Imaging Technology: a Revolution in the World of Imaging."
- **Luncheon Talk: SSDS DL Asad Abidi of UCLA on** "Alan Blumlien – the Greatest Circuit Designer."

Plenary Speaker: Dr. Christina Lampe-Onnerud, CEO and Founder, Boston Power

"Opportunities in Energy Storage due to the Paradigm Shift Fueled by the Mobile and Clean Tech Revolutions"

Energy security, economic growth and global warming are driving nations to develop electric vehicle technologies to reduce dependence on oil. Energy storage (batteries) will be critical to the success of this change. Utilities are also looking at energy storage throughout the grid to facilitate inclusion of renewable sources and improve the reliability and utilization of the existing grid infrastructure. Battery technology is reviewed with a focus on how improvements in lithium-ion technology will play a critical role in new transportation and utility systems.

Plenary Speaker: Dr. Satoru Fujikawa, Director of Strategic Semiconductor Development Center, Panasonic

"Three-Dimensional Imaging Technology: a Revolution in the World of Imaging."

In the 20th century, moving image technology underwent a steady stream of ground-breaking innovations, from the birth of motion pictures to the rise of television, to color, to HDTV, and beyond. Now in the 21st century, a revolutionary innovation is transforming moving imaging yet again, opening up the completely new and exciting world of 3D imaging. In this paper, we present the advanced digital technologies, 3D imaging systems, and system LSIs that coalesced to support this new generation of imaging.

Luncheon Talk: Prof. Asad Abidi, UCLA

"Alan Blumlein – the Greatest Circuit Designer"

Enjoy lunch and learn the accomplishments of one of the greatest geniuses of electronics whom history seems to have passed by. His accomplishments:

- Some of the earliest work on TV transmission
- Invention of stereo recording
- Invention of negative feedback amplifiers, independently of and possibly earlier than, Black
- Invention of the differential pair circuit
- Invention of the integrator circuit
- Invention of the cascode amplifier
- Invention of the voltage follower
- Invention of the most sensitive capacitance measuring bridge to date
- Invention of the practical tapped delay line filter (FIR filter)
- Key inventions in air-to-air radar
- He died in an air crash while flight testing a new radar system.

Short course#1: **Frequency synthesis and clock generation**

Organized by:

Andreia Cathelin, STMicroelectronics, Crolles, France

Shin'ichiro Mutoh, NTT, Tokyo, Japan

With support from Bora Nikolic, UC Berkeley, CA, USA

Morning

1. Basics of jitter and phase noise, by Asad Abidi, UCLA
2. Modeling/simulation of large signal phenomena in PLL, by Rick Poore, Agilent EEsof EDA
3. Architecture Trends and Requirements for Wireless RF PLLs, by Chih-Ming Hung, TI Dallas

Afternoon:

4. Low Power Frequency Synthesis using BAW/IC Integration, by Brian Otis, University of Washington, Seattle
5. Clocking techniques for high-speed wireline, by Jae-Yoon Sim, POSTECH Korea
6. Mm-wave PLL design, by Toshiya Mitomo, Corporate Research & Development Center, Toshiba Corp, Japan
7. Round table (all the speakers)

Short course#1: **Frequency synthesis and clock generation**

This year the short course on frequency synthesis and clock generation provides exciting presentations from 6 speakers, 3 from industry and 3 from academia. The first two presentations are theoretical ones, treating about basics of jitter and phase noise and then about modeling and simulations techniques of large signal phenomena in PLLs. The other four presentations treat each in detail a specific application field for frequency synthesis or clocking generation: all digital PLLs for wireless, low power frequency synthesis using MEMS/BAW resonators, clocking techniques for high speed wireline and finally PLL design for mm-Wave frequencies. At the end of the presentations, a 30 minutes round table will finally permit to conclude the day.

Short course #2: **Circuit Design for Technology Challenges**

Organized by:

Azeez Bhavnagarwala – IBM, Yorktown Heights, NY, USA

Koichi Nose – Renesas Electronics Corp., Japan

Morning:

1. CMOS Technology Trends, Ghavam Shahidi – IBM TJ Watson Research Center
2. CMOS Logic and Embedded Memory Design, Kevin Zhang - Intel
3. Design Methodology and Tools in an evolving CMOS Technology, Clive Bittlestone - Texas Instruments

Afternoon:

4. Analog/Mixed Signal Design in Digital CMOS, Dennis Fischette – AMD
5. Chip-Package-Co-design, Atsushi Nakamura – Renesas Electronics Corp.
6. Memory Design: Low Power DRAM Circuit & Interface Design, Yasuhiro Takai, Elpida
7. Memory Design: Disturbance and interference issues in NAND Flash design, Yeong T Lee, Samsung

Short course #2: **Circuit Design for Technology Challenges**

- MOS Technology is evolving in its manufacturing, non-silicon materials content and device structure to meet the increasingly severe power drain, performance and cost constraints imposed by emerging wireless and computing platforms in the presence of challenges imposed by variability, leakage and large SoC integration.
- This Short Course reviews the impact of these trends in MOS technology on circuit design, design methodology and CAD tools used by providing the design and technology communities a broad exposure to industry-best design practices in Logic, embedded Memory, Analog, SoC, Package, Memory Interface and Memory design that have emerged to meet these Technology challenges.

Rump Sessions

Organizers: JFE: Masanao Yamaoka (Hitachi) NAE: John Barth (IBM)

Circuits

Topics
C1: A role for VLSI in Green Technology? **Green technology is all the rage (as is quite obvious from the investment community). One way to reduce our overall carbon footprint is to rethink in a profound way how we produce, transport, store and consume energy in a profound way. Information technology (supported by advanced networks of semiconductor devices) may have to play a major role in that process. In this panel, we explore a number of visions from different business segments of how this may transpire, what is needed to really make it happen, and what the roadblocks may be.**
C2: Mixed Signal IP – Make vs. Buy **With the increasing use of foundries across the industry, the question of when to make IP vs. when to buy IP is becoming more important. This panel is focused on the chip manufacturer's choice of design vs buy for complex mixed-signal IP. Panelists will represent larger chip vendors, fab-less IP providers and mixed signal IP consumers.**

Rump Sessions

Organizers: JFE: Masanao Yamaoka (Hitachi) NAE: John Barth (IBM)

Joint

Topics
The International Technology Roadmap for Semiconductors (ITRS) charts future technology requirements and potential pathways for the industry to sustain the historical pace of improvement in *transistor performance and cost. These include the use of higher-permittivity gate dielectric materials,* high-mobility semiconductor channel materials, and non-classical structures to improve transistor drive current and scalability, and they vary depending on the application (high performance *vs. low operating* power *vs. low standby power). The issues of increasing MOSFET off-state leakage current and* performance variations with transistor scaling are fundamental challenges which will require joint Technology-Circuits solutions, in order for the industry to sustain the historical pace of improvement in *circuit performance and cost.* This panel discussion will aim to answer the following questions: • What do we expect to see in the next 10 years in terms of new devices and technologies? (Technologists will provide an ITRS-based perspective for future transistor improvement.) • Will these address the needs of the expected applications? (Circuit designers will describe driver applications and associated device requirements in terms of performance, power, cost, and design complexity.)

Rump Sessions

Organizers: JFE: Masanao Yamaoka (Hitachi) NAE: John Barth (IBM)

Circuits

Topics / Organizers	Moderators	Panelists
C1: A role for VLSI in Green Technology? **Jan Rabaey, Berkley** **Masahiro Nomura, Renesas Electronics Corp.**	**Jan Rabaey, Berkley**	**Christina Lampe-Onnerud, Boston-Power - Energy Storage** **Dave Freeman, Texas Instruments - Solar Systems** **Michio Kondo, AIST- Photovoltaics** **Yuji Nishibe, Toyota – Automotive**
C2: Mixed Signal IP – Make vs. Buy **Sreedhar Nataragan, TSMC** **Kazuhiko Kajigaya, Elpida Memory**	**Peter Rickert**	**Charlie Mater, VP Qualcomm** **ST Juang, TSMC, Senior Director IP Portfolio** **J. Boufarhat, AMD** **Simon Segars, GM ARM** **Mike Keating, VP Synopsis** **K. Arimoto, Renesas**
J: The Next Decade of VLSI Technology and Circuits – Are We on the Same Road? **Organizers (Tech.):** **Tsu-Jae King Liu (UC Berkeley)** **Shinya Yamakawa (Sony Corporation)** **Organizers (Circuit):** **Morgan Whatley (Cypress)** **Masanao Yamaoka (Hitachi)**	**Joel Dawson, MIT** **K Kuhn, Intel**	**Martin Izzard, TI, VP and Director. DSP Solutions R&D** **Cathal Phelan, Cypress, CTO** **David Robertson, ADI, VP Analog Technolgy** **Koichiro Ishibashi Ph.D, Circuit IP, SOC Design Technology** **M. Brillouet, CEA LETI** **T. Hiramoto, The University of Tokyo** **K. Imai, NECEL**

Highlight Papers (I)

Session: High-Resolution & High-Speed Data Converters

Paper: A 14b 200MS/s DAC with SFDR>78dBc, IM3<-83dBc and NSD<-163dBm/Hz across the whole Nyquist Band enabled by Dynamic-Mismatch Mapping

Lead Author: Yongjian Tang, Eindhoven University of Technology

Paper presents a 200 MS/s current-steering DAC with a novel dynamic-mismatch mapping technique that minimizes distortion caused by both static and dynamic current cell mismatches. Conventional techniques suppress distortion caused by static current cell mismatches, but do not suppress distortion caused by dynamic current cell mismatches. The DAC exhibits excellent high SFDR, low IM3, and low noise across the whole Nyquist band.

Session: Low-Power Nyquist ADCs.

Paper: 9-bit 150-MS/s 1.53mW Subranged SAR ADC in 90-nm.

Lead Author: Ying-Zu Lin, National Cheng Kung University

This demonstrates a significant increase in speed for a SAR ADC without losing accuracy. There's been a lot of talk about where the true benefit of submicron CMOS scaling will be, and it appears SAR is one of those positively affected areas. Because an SAR usually operates with just capacitors/switches and a comparator, it's largely unaffected by traditional analog problems of CMOS scaling. In this specific design, they precede a SAR with a frontend 3.5-bit flash, and they call this a "Subranged SAR". The architecture preserves all the benefits of a SAR, and the addition of a frontend flash comes with "digital corrections/redundancy" where comparator errors/offsets are tolerated. such architecture allows higher speed operation, and here they demonstrate a solid 9-bit 150-MS/s. This is driving very deeply into pipelined ADC neighborhood, and with less than 25-fJ/cs (femto joules per conversion step).

Highlight Papers (II)

Session: Clock Building Blocks

Paper: A programmable Phase Rotator based on Time-Modulated Injection-Locking

Lead Author: O'Mahoney, Intel

A high-precision, low DNL/ZNL programmable phase-rotator is realized in 45nm CMOS by modulating the injection point of an oscillator to achieve fine phase interpolation between coarse phases.

Session: PLL and CDR

Paper: A 9.2-12GHz, 90nm digital fractional-N synthesizer with stochastic TDC calibration and -35/-41dBc integrated phase noise in the 5/2.5GHz bands

Lead Author: Ravi, Intel

A new method to stochastically calibrate the non-linearities of the time-to-digital converter in a digital PLL that reduces spurs is proposed. A 90nm CMOS 9.2-12GHz digital fractional-N synthesizer using this method achieves better than -35dBc integrated phase noise in the 5-6GHz and spurs below -60dBc.

Session: Advanced Clock Generation

Paper: a 300GHz Fundamental Oscillator in 65nm CMOS Technology

Lead Author: Razavi, UCLA

Magnetic feedback from a differential pair to the core of the cross-coupled oscillator reduces the effect of device.

Highlight Papers (III)

Session: High-Speed On-Die Network & Processor Clocking

Paper: 2Tb/s 6x4 Mesh Network with DVFS and 2.3Tb/s/W router in 45nm CMOS

Lead Author: Praveen Salihundam, Intel

The paper presents a 6-by-4 mesh network-on-chip router fabricated in 45nm CMOS interconnecting 48 processor cores and 4 memory channels that achieve 2.3Tb/s/W. The design embodies dedicated voltage and frequency islands to enable workload-aware dynamic voltage frequency scaling.

Session: Advanced Wireline Tranceivers

Paper: A 5Gb/s Link with Clock edge matching and embedded common mode clock for low power interfaces

Lead Author: Zerbe, Rambus

Paper describes a 5Gb/s transceiver which uses a novel concept to minimize skew in the received clock, thereby removing a large amount of the source clock jitter.

Session: RF and uW Transceivers

Paper: A Quad-Band GSM/GPRS/EDGE SOC in 65nm CMOS

Lead Author: Darabi, Broadcom

A quad band 2.5GHz SOC integrations all of the RF, DSP, ARM, audio and other baseband processing functions into a single 65nm CMOS die.

Highlight Papers (IV)

Session: Digital Chip-to-Chip & On-Die Interfaces

Paper: 2.5kV isolation 35kV/us CMR 250Mbps 0.13mA/Mbps Digital Isolator in Standard CMOS with on-chip small transformer

Lead Author: Shunichi Kaeriyama, NEC

The paper presents the application of a on-chip transformer-based digital isolator for intelligent power-management capable of achieving 2.5kV isolation voltage and 34kV/us of common-mode-rejection in 5V standard CMOS.

Session: Digital Chip-to-Chip & On-Die Interfaces

Paper: A 1V 11fJ/Conversion-Step 10bit 10MS/s Asynchronous SAR ADC in 0.18μm CMOS

Author: Chun-Cheng Liu, National Cheng Kung University

A 10bit 10MS/s in 0.18um cmos at 10MS/s operation or higher, it's the best ever figure of merit (11 fJ/cs). Same author showed a 2010 ISSCC paper at 10bit 100MS/s, in 65nm cmos, with 15.5 fJ/cs.

Session: RF circuits and systems

Paper: An On-Chip Wideband and Low-Loss Duplexer for 3G/4G CMOS Radios

Lead Author: Mikhemar, UCLA

A wideband integrated duplexer supports most of the 3G/4G bands and achieves electrical performance which compares favorably with external passive devices.

Highlight Papers (V)

Session: Interference Robust RF Receivers

Paper: Quadrature Sampling Mixer Topology for SAW-Less GPS receivers in 0.18um CMOS.

Lead Author: Ikeuchi, Asahi Kasei Microdevices Corporation

This paper has a new mixer structure with 25% effective duty-cycle to filler interferers. Power is saved by stacking the VCO and the receiver itself in the supply voltage.

Session: BioSensors

Paper: A Digitally-Assisted Sensor Interface for Biomedical Applications

Lead Author: Bohorquez, MIT

This paper illustrates a digitally assisted blocker cancellation technique that is broadly applicable to biosensing systems.

Session: Digital Processors

Paper: Fine Grained Power analysis and Low-power techniques for a 128GFLOPS/58W SPARC64 VIIIfx Process for Petascale Computing

Lead Author: Okano, Fujitsu

This paper highlights the techniques required for high power parts using water cooling and other methods for a high-performance processor.

Highlight Papers (VI)

Session: Signal Processing for Wireless

Paper: a 1-190MSamples/s 8-64 Tap Energy-Efficient Reconfigurable FIR Filter for Multi-Mode Wireless Communication

Lead Author: Sheikh, UC Berkeley

The wide throughput range of the flexible DA FIR supports not on the targeted ATSC and DVB-T/H broadcast, GSM and UMTS 3G and WLAN 802.11/g/n standards, but also those requiring higher throughput rates at less than 2x the area- and energy-efficiency cost of dedicated filters.

Session: Resilient Digital Circuits

Paper: Resonant Supply Noise Canceller utilizing Parasitic Capacitance of Sleep Blocks

Lead Author: Jinmyoung Kim, Univ. of Tokyo

The paper applies a resonant supply noise canceller that utilizes the parasitic capacitance of sleep circuit blocks that achieves 43.3% & 12.5% supply noise reduction on abrupt voltage switching and abrupt wake-up of sleep block respectively.

Session: Medical and Vision Processors

Paper: Microwatt Embedded Processor Platform for Medical System-on-Chip Applications

Lead Author: Sridhara, Texas Instruments

This paper presents an ultra-low power medical application SoC that integrates an ARM processor with a 6T SRAM operating as low as 0.5V.

Conference Chairs

From left to right: Masayuki Mizuno, General Co-Chair, Ajith Amerasakera, Program Chair, Katsu Nakamura, General Chair, and Makoto Nagata, Program Co-Chair

Venue

The Symposia is returning to the Hilton Hawaiian Village in 2010. Located on Waikiki's widest stretch of beach, the Hilton Hawaiian Village Beach Resort & Spa features lush tropical gardens, waterfalls and exotic wildlife. For general information on the hotel, please go to Hilton Hawaiian Village.

For questions about hotel reservations you can reserve your room on-line at www.vlsisymposium.org

or you can contact:

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For registration and other information, visit the VLSI Symposia home page at: www.vlsisymposium.org or see more contact information in the SSCS Events Calendar.

Backup

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