2010 Symposium on VLSI Technology

The 2010 Symposium on VLSI Technology will be held at the Hilton Hawaiian Village in Honolulu, Hawaii, June 14-17, 2010. The Technology meeting begins with a short course for the VLSI Technology on June 14 entitled “Emerging Logic and Memory Technologies for VLSI Implementation”. There will be 22 technology sessions in the conference including a plenary session on the opening day of the Symposium with 2 plenary talks entitled “The Smart Grid and Key Research Technical Challenges” given by Michael G. Rosenfield of IBM and “SiC Technologies for Future Energy Electronics” given by Tsunenobu Kimoto of Kyoto University respectively. This year the VLSI Technology Symposium highlights three new focus areas covering forward-looking devices research beyond CMOS, heterogeneous integration and design enablement. The beyond-CMOS session explores spin-based and tunnel-based devices as potential alternative technology paths if CMOS hits a brick wall in scaling. There are four invited papers in the second new session exploring heterogeneous integration of compound semiconductors on silicon for extension of CMOS beyond conventional Si based technology and provides a direct path for more-than-Moore applications. The third new focus topic on design enablement has two sessions including 4 invited papers emphasizing the increasing need to exploit the synergy of cooperative technology and circuit design interaction as CMOS scales to 32nm and beyond.

Session 1
Plenary Session

The 2010 Plenary session will feature two invited speakers. The first plenary talk, “The Smart Grid and Key Research Technical Challenges” will be presented by Michael G. Rosenfield (Director, Smarter Energy, IBM T. J. Watson Research Center). The electric grid is transforming into an interconnected intelligent energy distribution system. The smart grid involves the merging of information and communication technologies with traditional energy delivery to enable the utilization of emerging renewable energy technologies such as wind and solar generation and increasing use of plug-in hybrid and electric vehicles. The presentation will focus on describing the smart grid and strategic technical challenges of enablement from a research perspective.

The second plenary talk, “SiC Technologies for Future Energy Electronics” will be presented by Tsunenobu Kimoto (Department of Electronic Science and Engineering, Kyoto University). High-efficiency electric power conversion is an essential technology for energy saving. The efficiency of power converters/inverters relies on the performance of power semiconductor devices employed in the power electronic systems. Silicon carbide (SiC) is a newly-emerging wide bandgap semiconductor, by which high-voltage, low-loss power devices can be realized owing to its superior properties. This paper reviews recent progress in SiC material and device technologies for power device applications. Benefits and remaining issues of SiC power devices are highlighted.

Session 2
Advanced CMOS 1
Chairpersons: O. Faynot, M. Masahara

The first 2 papers discuss FinFET device performance improvement and record FinFET SRAM cell demonstration.

Paper 2.1 presents a way to improve the FinFET device performance by using Aluminum implantation in order to reduce the access resistance.

Paper 2.2 reports the smallest SRAM cell size (0.06um2) ever demonstrated with FinFET and with a SIT process integration.

The third paper is dedicated to the demonstration of the world's first top-down CMOS ring oscillators fabricated with gate-all-around silicon nanowire FET with diameters down to 3nm.

The last paper reports a 0.099um2 SRAM cell also fabricated with FinFET, but with an EUV lithography used for contact and metal 1 lithographies.

Session 3
Reliability and Stability
Chairpersons: J. Cheek and S. Chung

Paper 3.1 demonstrates a product level aging monitor able to separate out contributions from negative bias instability (NBTI) and switching-activity dependent hot carrier stress in a 40nm CMOS process. While paper 3.2 examines the Vt stability of narrow width transistors in a high-k/metal gate 30nm FDSOI technology as a function of various high-k oxides. A mechanism for the Vt variability is proposed as well. In order to achieve low operating voltage (Vmin) in a 0.24μm² SRAM, paper 3.3 utilizes Hafnium doping at the poly/SiON interface to minimize NBTI shifts thereby improving cell stability. In addition, further improvement in SRAM cell stability is achieved with junction leakage reduction through optimization of the NiPt silicide process. Finally, paper 3.4 presents a Mg- or La- incorporated high-k/metal gate process and examines the origins of a anomalous Vt increase as well as suggestions on how to mitigate the observed increase.

Session 4
Advanced CMOS II
Chairpersons: M. Khare, H. Kurata

The first three papers in this session describe methods to leverage SiGe strain to enhance performance in both planar and 3D device structures.

Paper 4.1: The first paper demonstrates the shortest and narrowest (L = 20nm, W=30nm) n-FET and p-FET Trigate devices with compressively strained SiGe on insulator to achieve very high performance. Paper 4.2 discusses the utilization of strained SiGe channel on a planar (110) Silicon for improved p-FET and n-FET performance compared to planar (100) Si. This work proposes an extension of high mobility CMOS utilizing simple SiGe (110) <110> orientation while avoiding complex hybrid integration. Finally, Paper 4.3 studies layout dependence of SiGe planar transistors with channel strain conversion from biaxial in larger width to uniaxial in the narrow width devices. The enhanced drive current properties of such p-FET are also confirmed with nano-beam diffraction measurement and TCAD modeling.

The forth paper 4.4 in this session presents fully depleted SOI CMOS technology with

dual buried oxide for separate back bias control for n-FET and p-FET transistors. The effective back gate control of threshold voltage is demonstrated for CMOS devices which promise dual VT design with power gating capability.

Session 5
MRAM and X-Point RRAM
Chairpersons: K. Parekh, B.H. Lee

Papers in this session focus on MRAM (Spin-Transfer Torque Memory), and candidates for Resistive Random Access Memories.

Paper 5.1 explores MLC operation of a SPRAM with series connected MTJs. MTJs of different areas are connected in series to create multi level resistances by a combination of their magnetization directions.

Paper 5.2 discusses the adoption of a top-pinned stacking structure and an antiferromagnetic layer deposited over the MgO tunnel barrier to realize a 1T/1M structure relieved of driving power asymmetry and capable of reducing the cell area by about one half.

Paper 5.3 Investigates the data analysis and design requirements for thermal stability in STT-RAM. Thermal Stability is studied by various methods including dependence of write current on pulse width, switching probability distribution fitting, read disturb probability, and magnetic measurements. The results are compares with the thermal stability parameter predicted from spin-transfer torque theory.

The final paper in this session characterizes the resistive switching state of a Al/PCMO device. Based on this characterization, the authors propose feasibility of a cross point memory without selection device. Self-formed Schottky barrier by redox reaction at the Al/PCMO interface is used as the selection device. A simple cross point 4F2 memory array is proposed without additional processing steps.

Session 6
Ultra Thin Body FDSOI
Chairpersons: W. Xiong, T. Iwamatsu

Five excellent papers will be presented in this session

Paper 6.1 highlights the achievements made in CMOS with ultra-thin Si body (7nm) and ultra-thin BOX (10nm) substrate. Good AVT and SRAM cell characteristics are reported. Forward and reverse back biases were demonstrated to be effective in improving transistor drive current and managing leakage.

Paper 6.2 demonstrated co-integration of Localized-Silicon-on-Insulator (LSOI) devices with bulk IO on the same chip. Such process enables designer to enjoy the benefit of both SOI and bulk devices.

Paper 6.3 gives a detailed study of the impact of ground plane, buried oxide thickness and back biases on device performance. Significant Vt modulation with back bias and low AVT is reported. The paper also compares LSOI with UTBB SOI substrates.

Paper 6.4 evaluates the ultra-thin-body SOI scaling limits with full-band, quantum based device simulator. Paper found extremely strong surface roughness scattering will limit the scaling of such devices.

Paper 6.5 shows the capability of ultra-thin body SOI to provide multiple Vts (LVT, SVT, HVT) by using ground plane engineering and back bias. Both Ring Oscillator and SRAM cells were demonstrated.

Session 7
Process Technology
Chairpersons: Chorng-Ping Chang, Shigenori Hayashi

The five papers cover diverse issues on processing technology, such as effective oxide thickness (EOT) scaling, channel engineering for threshold voltage (Vt) variation reduction, mobility extraction and interface states improvement.

Paper 7.1 describes achieving zero interface oxide for EOT reduction by material engineering. The formation of LaCe-silicate gate dielectric enables a direct high-k/Si interface with reduction in both EOT and gate leakage (Jg). EOT of 0.64 nm with 0.65 A/cm2 is realized with good interface states density of ~1E11 cm-2/eV.

Paper 7.2 address an important issue of channel dopant diffusion control to suppress Vt variation. By utilizing light-absorber carbon layer and optimizing the power and pulse shape of flash lamp anneal (FLA), Vt variations of 1.3 mV-um and 1.2 mV-um are demonstrated with NMOS and PMOS respectively.

Paper 7.3 uses kinetic Monte Carlo (KMC) modeling to conduct pocket implant profile analysis on boron (B) clusters for NMOS. Laser anneal (LA) before spike rapid thermal anneal (RTA) achieves a 20% Vt variation improvement.

The next paper (7.4) showcases a new method for direction extraction of mobility and series resistance from a single, ultra-scaled device. This wafer level Hall mobility measurement methodology can be implemented with any convention prober (with small permanent magnet) with verifiable accuracy.

Finally, Paper 7.5 studies the phenomenon of improving SiO2/Si interface roughness under biaxial strain. The results reveals for the first time the strained Si (s-Si) is more immune to interface states generation, and with smaller interface roughness s-Si influences better device performances and reliability.

Session 8
RRAM Memory
Chairpersons: J. Lutze, S. Ohnishi

This session highlights advances in Resistive RAM development. The first paper, by Cheng et. al. of National Tsing Hua University, describes an RRAM structure with extremely low Set and Reset currents. The second paper, by Sakotsubo et. al. of NEC, describes a unipolar RRAM device with improved operating margin. The third paper, by Wang et. al. of Fudan University, describes an RRAM technology successfully integrated

into a standard logic process. The fourth and final paper, by Lin et. al. of Macronix, describes a novel solid electrolyte conducting bridge based RRAM technology.

Session 9
Variability
Chairpersons: R. Jammy, S. Yamakawa

This session highlights the increasing importance of variability as CMOS is scaled down to smaller geometries.

Paper 9.1 presented by Renesas Technology Corp. propose a statistical compact RTN (Random Telegraph Noise) model to accurately reproduce the experimental observation of Vth fluctuation. This is issue is becoming increasingly important as SRAMs are scaled down to smaller geometries.

Paper 9.2 presented by, MIRAI-Selete, The University of Tokyo, and Hiroshima City University analyses the cause of drain current local variability by decomposing into current variability components. In addition to VTH and Gm components, it is newly found that effects of “current onset” variability caused by channel potential fluctuations largely contribute to the current variability.

Paper 9.3 presented by Tohoku University, Japan investigates the energy distributions of traps which cause RTS noise using the array test pattern having a large number MOSFETs and compares the phenomena between both n-MOS and p-MOS FETs.

Paper 9.4 by University, Japan investigates the Vt variation in scaled FinFETs with Lg down to 25 nm and multi-FinFETs. It was found that the Vt of multi-FinFETs with the same gate area reduces with increasing the number of fins. FinFETs are increasingly being proposed as alternative to overcome the scaling road blocks in conventional planar CMOS technology

Session 10
3D Integration
Chairpersons: B. van Schravendijk, T. Tanaka

This session highlights the growing importance and technology challenges of scaling in the vertical direction through 3D integration as conventional “Moore” scaling in 2D may slow down.

Paper 10.1 by The University of Tokyo, Fujitsu Microelectronics Ltd., Dai Nippon Printing, and DISCO Corporation successfully thins
200-mm and 300-mm device wafers down to less than 10-μm demonstrating impact on both FRAM memory and CMOS logic.

Paper 10.2 by Panasonic Corporation revealed the mechanism of assembly stress in pad areas of the flip chip package by using high-k/metal gate Tr array.

Paper 10.3 is jointly presented by IMEC, Panasonic, Qualcomm, and Samsung demonstrates how 3D integration can alleviate the limitations CMOS scaling is facing provided that it preserves the integrity of FEOL and BEOL devices. The impact of wafer thinning and of the proximity of TSV on FEOL devices, BEOL structures, and mixed

signal circuit are reported for the first time for a High-k/Metal Gate first strained CMOS with low-k BEOL.

Paper 10.4 jointly presented by KAIST and ETRI demonstrate a spacer-free dopant-segregated-Schottky-barrier (DSSB) TFT SONOS is demonstrated for the application of 3D-TFT logic and flash memory devices. The DSSB TFT SONOS shows a good distribution of programmed VT by one-time programming with high-speed.

Session 11
Beyond CMOS
Chairpersons: Toshiro Hiramoto, Alan Seabaugh

This session highlights technologies with applications at the scaling limits of CMOS and beyond.

Researchers from NEC and the National Institute of Materials Science report on the high reliability of a nonvolatile programmable crossbar switch based on Cu ion bridging of a TaSiO electrolyte. The high reliability stems from the fact that stress is not accumulated under pulsed AC stressing. The technology is targeted for low power programmable-logic-device applications.

SpinFETs are field-effect transistors in which spin-polarized electrons are injected into the transistor channel through ferromagnetic contacts and collected at the drain also through a ferromagnetic contact. Purdue and Intel provide a performance assessment of the transistor at the 15 nm scale using numerical simulations showing delay, power, and area advantage over 15 nm CMOS.

Toshiba reports on Si-based spin-transfer-torque-switching MOSFETs consisting of a ferromagnetic electrode and a magnetic tunnel junction on the source and drain. The authors report measured dc transistor characteristics, read and write characteristics, and circuit simulations to show the enhanced functionality of the technology in nonvolatile and reconfigurable circuits.

Low-subthreshold-swing Si tunnel FETs are reported by a team of SEMATECH, Berkeley, and Texas State University achieving a subthreshold swing of 46 mV/ decade at a on-off ratio of 100 billion. The paper provides the first statistical analysis of tunnel FETs to support the sub-60-mV/decade subthreshold swing.

Session 12
NAND Memory
Chairpersons: J. Lutze, J.T. Moon

This session highlights advances in NAND Flash memory development. The first paper, by Park et. al. of Samsung, describes a state of the art 32nm 3 bit per cell NAND memory fabricated with a double patterning process. The second paper, by Seol et. al. of Samsung, describes a novel NAND cell structure with an additional nitride layer between the floating gate and IPD that is suitable for sub-20nm devices. The third paper, by Bloome et. al. of IMEC, introduces a dual layer poly/metal floating gate to enable scaling below 30nm. The fourth and final paper, by Lue et. al. of Macronix,

describes a 3D stacked NAND chain structure to enable high density and low cost memory.

Session 13
Design Enablement I
Chairpersons: K. Schruefer, C. Wann

This session is one of the three Focus Sessions of the Technology Symposium and includes five papers where the last three are invited papers, and is related to technology and circuit design interaction for advanced CMOS 32nm and beyond.

In paper 13.1, Qualcomm, presents for the first time, a 0.605μm2 dual core oxide (DCO) and dual Vdd 8T SRAM cell in triple gate oxide CMOS process for L1 cache high performance with 2x lower leakage compared to the standard 6T single oxide cell for mobile applications.

In the 2nd paper, Intel introduces its 32nm RF SOC technology with high-k/metal-gate triple-transistor architecture with record high performance and very low leakage devices to address advanced RF/mobile communications markets.

For 22nm and beyond, paper 13.3 by CMU demonstrates that using a limited set of pattern constructs can eliminate hotspot risk and can control systematic variability. Co-optimization with circuit design can eliminate or minimize density penalty on cell level and as well remove limitations imposed by complex design rules.

The fourth paper by Toshiba introduces novel circuit design and process technologies for leading-edge products focusing on two topics: (1) chip design optimization using extremely regular layout methodology, and (2) SiP (System in Package) with CoC (chip on chip) technology.

Finally, in paper 13.5 IBM reviews the technology features in the very recent and upcoming nodes and how they will impact circuit design, product performance, and migratability. It discusses the challenges and serious limitations that CMOS scaling will face and talk about some possible technology solutions that will address some of the challenges with an outlook that scaling is expected to continue to 11 nm (at least).

Session 14
Heterogeneous Integration
Chairpersons: R. Chau, K. Shibahara

This session focuses on the heterogeneous integration of non-silicon materials (e.g. III-V, Ge) on silicon substrate for advanced CMOS and beyond-CMOS applications. There are 5 papers in this session. The first paper from University of Tokyo talks about Ge and InGaAs as transistor channel materials for CMOS application. The second paper is from IBM and it discusses the suitability of III-V for CMOS and beyond-CMOS applications. The third paper from IMEC talks about the heterogeneous integration of GaN on large Si wafer for LED and high voltage power devices applications. The fourth paper (from ST) discusses the benefits versus disadvantages and challenges of using III-V as the transistor channel material. Finally the last paper from TSMC focuses on the benchmarking of the transistor performance of III-V transistor to that of silicon MOSFET.

Session 15
DRAM
Chairpersons : Carlos Mazure, Renichi Yamada

All four papers of this session focus on the floating body cell (FBC) as a memory candidate for node 15nm. Intel with two contributions studies the formation of the FBC cell with planar transistors and the impact of an additional back gate control. The first paper from Intel highlights the fact that avoiding implantation through the SOI layer by using pre-doped SOI substrates protects the top Si and a 10x increase in retention time can be achieved. With this approach future cells of 0.01μm² should be attainable with good retention characteristics.

IMEC and partners look at the FBC properties of FinFETs transistors on bulk and SOI as a function of fin width and channel length; and Hynix presents a vertical transistor concept for stand alone DRAM applications fabricated in 54nm DRAM technology compatible with low voltage operation.

Retention values around 1 second are low by stand alone DRAM standards but it could be enough for embedded FBC memories.

Session 16
Novel Devices
Chairpersons: C.P Chang, Yasunori Mochizuki

This session focuses on nano wires with the exception of the Samsung paper which presents a Tera Bit Cell Array Transistor (TCAT) for 3D NAND applications.
The first paper is the work of Toshiba aiming at the improvement of the current drive capability of nano wires. The main limiting factor that is to be addressed is the access source & drain resistance. The next paper from KAIST looks at nano wires for gateless memory application. The NPN nano wire they present exhibits 200msec retention times and offers the potential to achieve 1F² type of cells. Finally, the University of Tokyo studies the mobility dependence on the dimensions of nano wires over a wide range of nano wire widths, for channels below 10nm and nano wire thicknesses ranging from 4 to 10nm. A very exhaustive characterization of the nano wire mobility.

Session 17
Advanced CMOS III
Chairpersons: T. Skotnicki, Y. Akasaka

The four papers that constitute session #17, are discussing various new aspects gate stack for advanced CMOS.

Paper 17.1 gives a new insight into the Fermi level pinning phenomenon, emphasizing the crucial role of Carbon impurities. Based on this understanding, a new process is developed improving EOT-Jg characteristics and effective work function stability.

Paper 17.2 presents device results with ultra-scaled Tinv, down to Tinv~8Å using a gate-first dual Si/SiGe channel low-complexity integration approach. This process leads to

lower threshold voltages for both N- and P-MOS transistors, improved drive currents, and reduced variability.

Paper 17.3 reports on band-edge effective work functions for N- and P-MOS obtained using standard fab materials and processes in a gate-last scheme employing low-temperature anneals and selective cladding layers. Low Vt are demonstrated with N- and P-MOS transistors.

Paper 17.4 demonstrates for the first time a low cost, low complexity CMOS Hk/MG process for low-power applications with Vth controlled by gate Ion-Implantation (I/I) and High-k capping for NMOS and PMOS, respectively. Improved RO performance, with excellent uniformity and matching characteristics have been achieved without reliability degradation.

Session 18
Characterization and Modeling
Chairpersons: E. Kan, E. Morifuji

This session has four papers illustrating unique solutions to the increasing challenge of characterizing scaled geometry devices.

Paper 18.1 by NEC Electronics Corporation demonstrates a new accelerated testing scheme for detecting SRAM bit failure caused by random telegraph noise (RTN). By repeatedly monitoring the fail bit count (FBC) under a reduced margin operation condition, increasing trend of FBC along time was clearly observed, which is believed to be caused by RTN.

Paper 18.2 by University of Tokyo, MIRAI-Selete and STARC demonstrates the use of a special designed device-matrix-array (DMA) TEG of 16k bit SRAM cells. Static noise margins (SNM) and 6 transistors in cells are directly measured and their fluctuations are examined. It is found for the first time that one-side SNM follows the normal distribution up to ±4σ. It is also found that the cell stability is worse than circuit simulation using Vth of measured 6 transistors.

Paper 18.3 by CEA and TU Delft provides for the first an in-depth understanding of single dopant influence on NMOSFETs characteristics by linking low and room temperature transport. We demonstrate for gate length of 30 nm and below (channel length 10 nm) the presence of a single dopant dramatically alters the subthreshold behavior when the dopant is located in the middle of the channel. Moving the dopants away from the channel leads to enhanced variability above Vt.

Paper 18.4 by IMEC and KU demonstrates atom probe tomography (APT) in conjunction with scanning spreading resistance microscopy (SSRM) for the first time to profile dopant and carrier distributions in FinFET-based devices with sub-nanometer resolution. These two techniques together provide information on the degree of conformality, the dose retention and the dopant activation. These results are also compared with a methodology involving secondary ion mass spectrometry (SIMS).

Session 19
PCRAM

Chairpersons: K. Parekh, H. Miyake

Papers in this session focus on Phase Change Random Access Memory technology

Paper 19.1 focuses on overcoming thermal-induced erase failures of unselected cells through optimized programming. This approach is aimed at achieving a highly scalable architecture capable of 16nm 4F2 PCM

Paper 19.2 proposes an integrated method to realize MLC in PRAM at 45nm. Programming techniques include 2bit write to enhance write and verify speed and 3 –cell reference schemes to deal with variation from resistance and temp induced shifts.

Paper 19.3 describes the integration of a confined cell PRAM (7.5nm X 17nm) which is scalable to sub 20nm with 4F2 or smaller cell architecture. Sb rich GST phase change material is used to for high speed operation below 30ns, with high predicted endurance and 4.5years data retention at 85'C making it a candidate for DRAM applications.

The final paper in this session demonstrates a Cu-ion motion based access device using Mixed Ionic Electronic Conduction (MIEC) materials. This novel access devices is seen as a compatible device with <400'C BEOL and an enabler for 3D stacked PCM.

Session 20
Ge MOSFETs
Co-chairs: Raj Jammy, Kentaro Shibahara

This session is comprised of four papers which describe different approaches to enhancing the performance of germanium (Ge) MOSFETs.

The first three papers focus on gate-stack process and material improvements. Paper 20.1 discusses the formation of nearly perfect GeO_2/Ge gate stacks via high-pressure oxidation of Ge and low-temperature oxygen annealing, resulting in the highest reported electron mobility for a Ge n-channel MOSFET. Paper 20.2 demonstrates the scalability of a $LaAlO_3$/$SrGe_x$/Ge gate stack toward 1nm equivalent oxide thickness for improved transistor drive current, with low gate leakage. Paper 20.3 proposes the use of a Ge nitride interfacial layer to achieve low interface trap density for improved Ge MOSFET performance.

Lastly, Paper 20.4 studies high-field transport in short-channel (70nm) Ge p-channel MOSFETs and shows that strain can be used to enhance drive current by 1.4x in the ballistic regime.

Session 21
Design Enablement II
Chairpersons: K. Schruefer, C. Wann

This session is the second of the two Focus Sessions of the Technology Symposium on Design Enablement and includes five papers where the last three are invited papers, and is related to technology and circuit design interaction for advanced CMOS 32nm and beyond.

In paper 21.1, Toshiba presents the world's first monolithically integrated TFT-SRAM configuration circuits over 9-layers of Cu-interconnect CMOS successfully fabricated for 3D-FPGA to overcome conventional CMOS scaling.

In the second paper 21.2, Texas Instruments introduces novel and cost-effective integration schemes with high-performance analog and high voltage components to enable SOC designs in advanced CMOS technologies. All of these components are integrated in a standard digital CMOS process without cost adders.

Qualcomm highlights in paper 21.3 how a multi-design strategy for Smart Mobile Devices as Complex Systems influenced architecture, device/circuit and package solutions for 28nm and beyond, in the face of growing process cost, and from an Integrated Fabless Manufacturer (IFM)'s perspective.

The fourth paper 21.4, TSMC, discusses technology and design challenges at 28nm and 20nm technology nodes, and provides solutions as key enablement for designers to effectively overcome those challenges.

Finally, in paper 13.5 Intel describes design challenges in utilizing advanced features, such as fully depleted transistors, compound semiconductors, embedded memory, and 3D integration, and evaluates their benefits.

Session 22
Exploratory Devices
Chairpersons: Alan Seabaugh, Shinichi Takagi

New channel materials, graphene, carbon nanotubes, GaAs, and InGaAs, are being employed to extend the performance of silicon MOSFETs.

A significant advance in graphene growth has enabled IBM researchers to transfer single and double graphene layers with greater than 1 square centimeter areas onto Si for transistor development. This has enabled the first study of channel length scaling in the range from 90 to 5000 nm and the revelation of a new short-channel effect which must be addressed.

Taiwan researchers from the National University of Singapore, TSMC, the National Nano Device Laboratory, and the National Chiao-Tung University demonstrate a self-aligned salicide-like process for GaAs MOSFETs utilizing NiGeSi. Development of self-aligned processes is key to utilizing III-V materials in logic applications.

Researchers from the University of Tokyo, the National Institute of Advanced Industrial Science and Technology, and Sumitomo demonstrate InGaAs-on-insulator MOSFETs with an insulator formed by atomic layer deposition of aluminum oxide. This insulator forms a more abrupt interface to the InGaAs channel than silicon dioxide and results in higher channel mobility.

To construct a VLSI system using carbon nanotubes - a process is needed to select semiconducting from metallic nanotubes because the metallic tubes cannot be turned off. Stanford engineers demonstrate an electrical method for removing the metallic nanotubes from aligned blocks of nanotubes, and prove the process by construction of inverters and NAND gates. The process can be extended to wafer scale.