JOINT TECHNOLOGY/CIRCUITS
RUMP SESSION
Tuesday, June 15
8:00 p.m – 10:00 p.m.

RJ1: The Next Decade of VLSI Technology and Circuits – Are We on the Same Road?

Organizers:

Circuits	*Technology*
M. Whately, Cypress	T-J King Liu, University of California, Berkeley
M. Yamaoka, Hitachi	S. Yamakawa, Sony Corp.

Moderators: J. Dawson, Massachusetts Institute of Technology
K. Kuhn, Intel

The International Technology Roadmap for Semiconductors (ITRS) charts future technology requirements and potential pathways for the industry to sustain the historical pace of improvement in *transistor* performance and cost. These include the use of higher-permittivity gate dielectric materials, high-mobility semiconductor channel materials, and non-classical structures to improve transistor drive current and scalability, and they vary depending on the application (high performance *vs.* low operating power *vs.* low standby power). The issues of increasing MOSFET off-state leakage current and performance variations with transistor scaling are fundamental challenges which will require joint Technology-Circuits solutions, in order for the industry to sustain the historical pace of improvement in *circuit* performance and cost.

This panel discussion will aim to answer the following questions:

- What do we expect to see in the next 10 years in terms of new devices and technologies? (Technologists will provide an ITRS-based perspective for future transistor improvement.)
- Will these address the needs of the expected applications? (Circuit designers will describe driver applications and associated device requirements in terms of performance, power, cost, and design complexity.)

Panelists:

M. Brillouet, CEA LETI
T. Hiramoto, University of Tokyo
K. Imai, NECEL
K. Ishibashi, Renesas Electronics Corp.
M. Izzard, Texas Instruments, Inc.
C. Phelan, Cypress Semiconductor Corp.
D. Robertson, Analog Devices, Inc.

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R1 What Will End Moore's Law?

Moderators:

Hidemi Ishiuchi, Toshiba
Malgorzata Jurczak, IMEC

Moore's Law of exponentially increasing transistor count per chip over time has prevailed despite the challenges of increasing power density and variability for deep-sub-micron CMOS technologies. Some argue that in fact Moore's Law ended at the 90 nm node, beyond which the pace of circuit performance gains slowed. Others hold that the essence of Moore's Law, that is decreasing cost per transistor, has been maintained. As new materials and non-classical transistor structures are adopted, even this may be in jeopardy, however. This panel discussion will discuss various reasons why Moore's Law will end, and describe approaches to delay or circumvent them. These include the following:

- Lithography: It may be too costly to print features at sub-16nm half-pitch.
- Device physics: Quantum-mechanical tunneling and voltage-scaling limits can result in unacceptably high power densities and therefore limit device pitch scaling.
- Economics: The semiconductor market will not grow at a pace sufficient to provide the economies of scale needed to sustain Moore's Law.

Finally, this panel will consider possible replacements for Moore's Law to set the cadence for the semiconductor industry after 2020.

Panelists:

Bill Arnold, ASML
Serge Biesemans, IMEC
Robert Chau, Intel
Scott Kramer, SEMATECH
Hirofumi Shinohara, STARC
Toshiharu Watanabe, Toshiba

R2 The Future of Embedded Memory

Moderators:

Leland Chang, IBM T. J. Watson Research Center
Tetsuo Endoh, Tohoku University

Embedded memory is a key component in determining the speed, power, reliability, and yield of integrated circuits. For decades, six-transistor (6T-) SRAM scaled in accordance with Moore's Law and served well as the primary embedded memory option. However, continued scaling of 6T-SRAM brings about fundamental challenges such as transistor mismatch due to Vth fluctuation, which, particularly in conjunction with voltage scaling, can result in severe degradation of read and write operating margins. While the industry has worked in earnest to cope with SRAM scaling issues, alternative approaches have also been widely investigated.

In recent years, embedded DRAM has gained acceptance, even for high performance applications, and emerging technologies such as embedded Flash, MRAM, SP-RAM, FeRAM, PCM, ReRAM, FBC-RAM, and T-RAM have all made significant strides. This panel discussion will look towards future embedded memory technology in the 22/16 nm era and beyond to answer the following questions:

- In this time frame, what do we need memory to do (e.g. density, performance, power, non-volatility) in embedded applications? What might we be able to trade off to achieve these goals?
- Will SRAM ever be displaced as the embedded memory of choice?
- Which emerging technologies are practically suited for anticipated embedded memory needs? What challenges are involved in developing these technologies?

Panelists:

Takahiro Hanyu, Tohoku University
Subramanian Iyer, IBM Corporation
Naoki Kasai, NEC
Alfonso Maurelli, STMicroelectronics
Koji Nii, Renesas Electronics Corp.
Yoshio Nishi, Stanford University