SESSION 10 – TAPA III
3D Integration

Wednesday, June 16, 10:25 a.m.
Chairpersons: B. van Schravendijk, Novellus Systems, Inc.
T. Tanaka, Tohoku University

10.1 - 10:25 a.m.
Development of Sub 10-µm Ultra-ThinningTechnology Using Device Wafers for 3D Manufacturing of Terabit Memory, N. Maeda, Y.S. Kim*, Y. Hikosaka*, T. Eshita*, H. Kitada, K. Fujimoto**, Y. Mizushima^, K. Suzuki**, T. Nakamura^, A. Kawai^^, K. Arai^^, T. Ohba, The University of Tokyo, *Fujitsu Microelectronics Ltd., **Dai Nippon Printing, ^Fujitsu Laboratories Ltd., ^^DISCO Corporation, Japan

200-mm and 300-mm device wafers were successfully thinned down to less than 10-µm. A 200-nm non-crystalline layer remaining Backgrind process was partially removed by Ultra Poligrind process, or was completely removed with either CMP or Dry Polish. For FRAM device wafers thinned down to 9-µm, switching charge showed no change by thinning. CMOS logic device wafers thinned to 7-µm indicated neither change in Ion current nor junction leakage.

10.2 - 10:50 a.m.
Assembly-Stress-Mechanism in Pad Areas on High-k/Metal Gate Transistors, Y. Ota, F. Itoh, K. Ishikawa, K. Hagihara, T. Matsumoto, T. Iwase, Y. Itoh, H. Hirano, Panasonic Corporation, Japan

We have revealed the mechanism of assembly stress in pad areas of the flip chip package by using high-k/metal gate Tr array. We have also showed the temperature dependence of assembly stress and revealed its mechanism. Based on our investigation, we propose a new structure and expect to reduce assembly stress by 30%.

10.3 - 11:15 a.m.
Impact of Thinning and Through Silicon Via Proximity on High-k / Metal Gate First CMOS Performance, A. Mercha, A. Redolfi, M. Stucchi, N. Minas, J. Van Olmen, S. Thangaraju, D. Velenis, S. Domae*, Y. Yang^^, G. Katti^^, R. Labie, C. Okoro^^, M. Zhao, P. Asimakopoulos, I. De Wolf, T. Chiarella, T. Schram, E. Rohr, A. Van Ammel, A. Jourdain, W. Ruythooren, S. Armini, A. Radisic, H. Philipsen, N. Heylen, M. Kostermans, P. Jaenen, E. Sleeckx, D. Sabuncuoglu Tezcan, I. Debusschere, P. Soussan, D. Perry**, G. Van der Plas, J.H. Cho^, P. Marchal, Y. Travaly, E. Beyne, S. Biesemans, B. Swinnen, IMEC, *Panasonic, ** Qualcomm, ^Samsung, ^^IMEC and KU Leuven, Belgium

3D integration can alleviate the limitations CMOS scaling is facing provided that it preserves the integrity of FEOL and BEOL devices. The impact of wafer thinning and of the proximity of TSV on FEOL devices, BEOL structures, and mixed signal circuit are reported for the first time for a High-k/Metal Gate first strained CMOS with low-k BEOL. The impact of the stress on a sensitive circuit is used to define a keep out area.

10.4 - 11:40 a.m.
A Novel TFT with a Laterally Engineered Bandgap for of 3D Logic and Flash Memory, S.-J. Choi, J.-W. Han, S. Kim, D.-I. Moon, M. Jang*, Y.-K. Choi, KAIST, *ETRI, Korea

A spacer-free dopant-segregated-Schottky-barrier (DSSB) TFT SONOS is demonstrated for the application of 3D-TFT logic and flash memory devices. The DSSB TFT SONOS shows a good distribution of programmed VT by one-time programming with high-speed (a VT shift of 2.9V @ 32ns) due to the inherent DSSB nature, which is not also affected by grain boundaries. Moreover, the program speed is accelerated by reduction of the fin width owing to the enhanced field.