SESSION 11 – TAPA II
Beyond CMOS

Wednesday, June 16, 1:30 p.m.
Chairpersons: A. Seabaugh, Notre Dame University
T. Hiramoto, University of Tokyo

11.1 - 1:30 p.m.
Reliable Solid-Electrolyte Crossbar Switch for Programmable Logic Device, N. Banno, T. Sakamoto, M. Tada, M. Miyamura, Y. Yabe, Y. Saito, S. Ishida, K. Okamoto, H. Hada, N. Kasai, N. Iguchi*, M. Aono*, NEC Corp., *NIMS, Japan

Solid-electrolyte crossbar switch (namely NanoBridge) with low programming current of 420μA and highly reliable ON state against pulsed-alternating current stress (>10years, 150 degrees C) is demonstrated under actual operating conditions of a programmable logic device. The high reliability under AC originates from the fact that the stress induced by Cu ion migration at a negative bias is recovered by a positive bias. NanoBridge is applicable in a scaled-down, nonvolatile PLD for hp28 and beyond.

11.2 - 1:55 p.m.
Realistic Spin-FET Performance Assessment for Reconfigurable Logic Circuits, Y. Gao, C. Augustine, D. Nikonov*, K. Roy, M. Lundstrom, Purdue University, *Intel, USA

A Numerical simulation of spin field-effect transistor including for the first time the effects of channel spin relaxation and interface tunnel barriers is implemented. Magnetoresistance ratio is found to be lower than earlier predictions, but can be increased by adjusting contact parameters and inserting tunnel barriers. Reconfigurable circuits with spinFETs shows ~7X, ~32X, ~6X improvements in delay, power, area respectively against 15nm CMOS. Moreover, spinFET can function as sleep transistor to reduce leakage by >10000X.

11.3 - 2:20 p.m.
Reconfigurable Characteristics of Spintronics-based MOSFETs for Nonvolatile Integrated Circuits, T. Inokuchi, T. Marukame, T. Tanamoto, H. Sugiyama, M. Ishikawa, Y. Saito, Toshiba Corporation, Japan

Reconfigurability of a novel spintronics-based MOSFET; “STS-MOSFET” was successfully realized in transport properties. The device showed magnetocurrent (MC) and write characteristics with the endurance of over 10^5 cycles. It was clarified that the read and write characteristics can be improved by choosing connection configurations of STS-MOSFETs. Large scale circuit simulations for FPGAs revealed that the critical path delay is significantly improved by using STS-MOSFETs. The overall properties show great potentialities for future reconfigurable integrated circuits.

11.4 - 2:45 p.m.
Si Tunnel Transistors with a Novel Silicided Source and 46mV/dec Swing, K. Jeon, W.-Y. Loh*, P. Patel, C.Y. Kang*, J. Oh*, A. Bowonder, C. Park*, C.S. Park*, C. Smith*, P. Majhi*, H.-H. Tseng**, R. Jammy*, T.-J. King Liu, C. Hu, *SEMATECH, **Texas State University The University of California, Berkeley, USA

We report a novel tunneling field effect transistor fabricated with a high-k/metal gate stack and using nickel silicide to create a special field-enhancing geometry and high dopant density by dopant segregation. It produces steep subthreshold swing of 46mV/dec and high ION/IOFF ratio (~1E8). For the first time convincing statistical evidence of sub-60mV/dec SS is presented. More than 30% of the devices show sub-60mV/dec SS after systemic data quality checks that screen out unreliable data.