SESSION 12 – TAPA III
NAND Flash Memory

Wednesday, June 16, 1:30 p.m.
Chairpersons: J. Lutze, Sandisk Corp.
J.T. Moon, Samsung Electronics Co., Ltd.

12.1 - 1:30 p.m.
32nm 3-Bit 32Gb NAND Flash Memory with DPT (Double Patterning Technology) Process for Mass Production, B.T. Park, J.H. Song, E.S. Cho, S.W. Hong, J.Y. Kim, Y. J. Choi, Y.S. Kim, S.J. Lee, C.K. Lee, D.W. Kang, D.J. Lee, B.T. Kim, Y.J. Choi, W.K. Lee, J.-H. Choi, K.-D. Suh*, T.-S. Jung, Samsung Electronics, *STET, Korea

32nm 3-bit 32Gb NAND Flash Memory for mass production has been successfully developed for the first time. To shorten the development time and lower the cost, one side double patterning technology in a gate direction and the minimum number of spare blocks have been adopted. Additionally, considering endurance and data retention of cell characteristics, the optimal gate and active lengths are fixed in a stage of device design.

12.2 - 1:55 p.m.
A New Floating Gate Cell Structure with a Silicon-nitride Cap Layer for Sub-20 nm NAND Flash Memory, K.S. Seol, H. Kang, J. Lee, H. Kim, B. Cho, D. Lee, Y.-L. Choi, N.-H. Ju, C. Choi, S. Hur, J. Choi, C. Chung, Samsung Electronics

A new cell structure of NAND memory devices, which employs an additional nitride layer between the top of a floating gate (FG) and inter-poly dielectrics (IPD), is devised to lesson a high electric field on the FG top edges during program. The cell structure is proved to be promising in sub-20 nm NAND generation in terms of larger program window, better endurance, and more robust data retention, which are obtained by decreasing a leakage current of IPD relating with the electric field on the FG top edges.

12.3 - 2:20 p.m.
Novel Dual Layer Floating Gate Structure as Enabler of Fully Planar Flash Memory, P. Blomme, M.Rosmeulen, A. Cacciato, M. Kostermans, C. Vrancken, S. Van Aerde*, T. Schram, I. Debusschere, M. Jurczak, J. Van Houdt, IMEC, *ASM, Belgium

Flash pitch scaling will lead to cells for which the wordline no longer fits between the floating gates, which results in loss of sidewall coupling, causing unacceptable program saturation due to IPD leakage. We present a dual layer poly/metal floating gate (FG) memory device avoiding this saturation and demonstrate +4V programming above the fresh level in a fully planar cell without sidewall coupling using an Al2O3 IPD. The data retention at 200C and cycling performance up to 100k cycles are similar to cells with poly FG.

12.4 - 2:45 p.m.
A Highly Scalable 8-Layer 3D Vertical-Gate (VG) TFT NAND Flash Using Junction-Free Buried Channel BE-SONOS Device, H.-T. Lue, T.-H. Hsu, Y.-H. Hsiao, S.P. Hong, M.T. Wu, F.H. Hsu, N.Z. Lien, S.-Y. Wang, J.-Y. Hsieh, L.-W. Yang, T. Yang, K.-C. Chen, K.-Y. Hsieh, C.-Y. Lu, Macronix International Co., Ltd, Taiwan

An 8-layer, 75 nm half-pitch, 3D stackable vertical-gate (VG) TFT BE-SONOS NAND Flash and the associated NAND array characteristics are demonstrated in this work. We propose a buried-channel (n-type well) device to improve the read current of TFT NAND, and it also allows the junction-free structure which is particularly important for 3D stackable devices. Large self-boosting disturb-free memory window

(6V) can be obtained in our device, and for the first time the “Z-interference” between adjacent vertical layers is studied.