SESSION 13 – TAPA II
Design Enablement I

Wednesday, June 16, 3:35 p.m.
Chairpersons: K. Schruefer, Infineon Technologies
C. Wann, Taiwan Semiconductor Manufacturing Company

13.1 - 3:35 p.m.
A Dual Core Oxide 8T SRAM Cell with Low Vccmin and Dual Voltage Supplies in 45nm Triple Gate Oxide and Multi Vt CMOS for Very High Performance yet Low Leakage Mobile SoC Applications, P. Liu, J. Wang, M. Phan, M. Garg, R. Zhang, A. Cassier, L. Chua-Eoan, B. Andreev, S. Weyland, S. Ekbote, M. Han, J. Fischer, G. Yeap, P.-W. Wang*, Q. Li*, C.S. Hou*, S.B. Lee*, Y.F. Wang*, S.S. Lin*, M. Cao*, Y.J. Mii*, Qualcomm, USA, *TSMC, Taiwan

For the first time, 0.605µm2 dual core oxide (DCO) and dual Vdd 8T SRAM cell in 45LPG triple gate oxide CMOS process for L1 cache high performance low leakage mobile applications. Compared to traditional single-end 8T cell, DCO 8T cell showed only half standby leakage and lower Vccmin with the same performance. DCO boundary was optimized to achieve robust Vccmin, process margin and reliability. 45LPG thin core transistors and the DCO 8T SRAM are able to achieve 1.5GHz speed with ~500mW at 0.9V and a low Vccmin of 0.6V.

13.2 - 3:50 p.m.
A 32nm Low Power RF CMOS SOC Technology Featuring High-k/Metal Gate, P. VanDerVoorn, M. Agostinelli, S.-J. Choi, G. Curello, H. Deshpande, M. A. El-Tanani, W. Hafez, U. Jalan, L. Janbay, M. Kang, K.-J. Koh, K. Komeyli, H. Lakdawala, J. Lin, N. Lindert, S. Mudanai, J. Park, K. Phoa, A. Rahman, J. Rizk, L. Rockford, G. Sacks, K. Soumyanath, H. Tashiro, S. Taylor, C. Tsai, H. Xu, J. Xu, L. Yang, I. Young, J.-Y. Yeh, J. Yip, P. Bai, C.-H. Jan, Intel Corporation

A 32nm RF SOC technology is developed with high-k/metal-gate triple-transistor architecture simultaneously offering devices with high performance and very low leakage to address advanced RF/mobile communications markets. A high performance NMOS achieves an fT of 420GHz. Concurrently, a low leakage 30pA/um NMOS achieves an fT of 218GHz. Deep-nwell/guard rings improve noise isolation by >50dB. High Q inductors, >7V breakdown voltage power amplifier transistors, varactors, and precision passives are also presented.

13.3 – 4:15 p.m.
Enabling Application-Specific Integrated Circuits on Limited Pattern Constructs (Invited), D. Morris, V. Rovner, L. Pileggi, A. Strojwas, K. Vaidyanathan, Carnegie Mellon University, USA

Implementing sub-22nm designs using a limited set of pattern constructs can eliminate hotspot risk and can control systematic variability. Pattern regularity can incur a cell-level density penalty that is minimized or eliminated by co-optimization with circuits. More importantly, design with a limited set of pattern constructs can remove the limitations imposed by complex design rules, thus facilitating flexible synthesis of logic and memory blocks in place of hard IP.

13.4 – 4:40 p.m.
Novel Circuit Design and Process Technology for Leading-Edge Products (Invited), K. Miyamoto, A. Strojwas*, E. Hosomi, M. Ooida**, H. Ezawa, M. Fukuda, Y. Matsubara and K. Numata, Toshiba Corporation, *PDF Solutions, Inc,- **J-Devices Corporation, Japan

Achieving power, performance, yield and cost scaling targets at leading edge technology nodes has become significantly more challenging. Success is driven by making the optimal combination of process, design, and package decisions [1]. In this paper, we report novel circuit design and process technologies

for leading-edge products. We focus on two topics: (1) chip design optimization using extremely regular layout methodology, and (2) SiP (System in Package) with CoC (chip on chip) [2] for 40nm technology node [3] products.

13.5 – 5:05 p.m.
Design-Technology Interaction for Post-32 nm Node CMOS Technologies (Invited), G. Shahidi, IBM Thomas J. Watson Research Center, USA

This paper will review the technology features in the recent and upcoming nodes and how they will impact circuit design, product performance, and migratability. It will cover the challenges and serious limitations that we will face in FEOL (increased leakage, loss of body effect), BEOL (RC, electro-migration), lithography (ever more complex design rules), and power management (end of frequency scaling, very high device count). We will talk about some possible technology solutions that will address some of the above challenges (disruptive device technologies, increased number of BEOL levels, and migration to lower voltages). Net is that scaling is expected to continue to 11 nm (at least). Design is expected to become significantly more complex.