SESSION 14 – TAPA III
Heterogeneous Integration

Wednesday, June 16, 3:25 p.m.
Chairpersons: R. Chau, Intel Corp.
K. Shibahara, Hiroshima University

14.1 – 3:25 p.m.
III-V/Ge CMOS Technologies on Si Platform (Invited), S. Takagi and M. Takenaka, The University of Tokyo, Japan

III-V/Ge CMOS on Si platform, realized by heterogeneous integration, is expected to provide a variety of applications from high speed logic CMOS to versatile SoC chips, where various functional devices can be co-integrated. Among them, we are currently pursuing high speed/low power logic CMOS using III-V/Ge channels. While many critical issues have been well recognized for them, we present possible solutions to break through these difficulties in this presentation.

14.2 – 3:50 p.m.
III-V: Replacing Si or More than Moore? (Invited), Y. Sun, IBM Thomas J. Watson Research Center, USA

Frequency scaling is coming to an end because of thermal limits as shown in Fig. 1. As an alternative nFET channel material, III-V compound semiconductor has been under intensive investigation in the recent years, hope to provide higher performance and lower power devices. In this paper, we review the status of current III-V research, and discuss the challenges and opportunities for “Moore” and “more than Moore” applications.

14.3 – 4:15 p.m.
GaN-on-Si: A Scalable Material System to Realize Cost Effective Next-Generation Solid State Lighting and Power Devices (Invited), S. Decoutere, H. Osman, J. Dekoster, B. Dutta, S. Biesemans, IMEC, Belgium

Over the last decade Gallium Nitride and its compound semiconductor derivatives that belong to the III-V system have demonstrated significant performance advantages in the area of light emitting diodes and high power devices. These have been enabled by their intrinsic wide band-gap of around 3.4eV which manifest itself as enabling efficient light emission in the blue and green, as well as excellent transport properties (2DEG mobility of 1000-2000cm2/Vs) enabling high power & frequency transport devices which can operate at high temperature with high breakdown voltages, enabling an entire set of devices to address power efficiency.

14.4 – 4:40 p.m.
How Can High Mobility Channel Materials Boost or Degrade Performance in Advanced CMOS (Invited), T. Skotnicki and F. Boeuf, STMicroelectronics, France

Big hopes are still placed in high mobility materials such as III-V compound semiconductors. The key new elements that may moderate this belief are: degradation of DIBL, subthreshold slope and gate capacitance due to larger dielectric constant and smaller density of states in III-V materials. We will show how DIBL plays directly on performance, especially in LP technologies. This effect is now for the first time taken into account along with all other degradation sources associated with III-V channels. As a result, the gain in performance turns out to be much smaller than the expected 2X, and even become negative. This analysis also shows in which applications and conditions, the III-V channels exhibit their strengths the best.

14.5 – 5:05 p.m.

Classification and Benchmarking of III-V MOSFETs for CMOS (Invited), M. Passlack, G. Doornbos, C. Wann, Y.C. Sun, TSMC, Belgium, Taiwan

A classification scheme for III-V MOSFETs for future CMOS is proposed and n-channel devices are benchmarked both within the group of III-V MOSFETs and in comparison with state-of-the-art silicon MOSFETs. Metrics which are based on the first derivative of drain current (Id) vs gate voltage (Vgs) are found to be most suitable for benchmarking technologies of widely diverging maturity level. Although recently reported III-V MOSFETs exhibit markedly improved performance, they still lag state-of the-art Si MOSFETs. However, Schottky gate III-V devices with an InAs channel layer already outperform silicon MOSFETs today.