SESSION 15 – TAPA II
**DRAM**

Thursday, June 17, 8:30 a.m.
Chairpersons: C. Mazure, Soitec Group
R. Yamada, Hitachi Research Institute

**15.1 - 8:30 a.m.**
**Integration of Back-Gate Doping for 15-nm Node Floating Body Cell (FBC) Memory,** I. Ban, U. Avci, D. Kencke, P. Tolchinsky, P. Chang, Intel Corp, USA

Key process features of a scaled FBC memory fabricated on 25-nm undoped Si and 10-nm BOX SOI substrates are presented. Back-Gate doping process is revealed to be a critical part of the FBC integration. BG dopant loss due to oxidation and high-temperature processes is minimized to enable high performance at scaled diffusion widths. Memory retention of over 1 sec (@ 3-µA sensing window) in scaled cells (Lg=50 nm, W=85 nm) is suitable for 15-nm node.

**15.2 - 8:55 a.m.**
**A Low-Voltage Biasing Scheme for Aggressively Scaled Bulk FinFET 1T-DRAM Featuring 10s Retention at 85°C,** N. Collaert, M. Aoulaiche, B. De Wachter, M. Rakowski, A. Redolfi, S. Brus, A. De Keersgieter, N. Horiguchi, L. Altimime, M. Jurczak, IMEC, Belgium

Retention times up to 10s at 85°C can be achieved for bulk FinFET 1T-DRAM devices using an optimized biasing scheme which targets the storage of electrons in the fin. The impact of the ground plane doping is investigated and finally the read-out scheme is also demonstrated on SOI FinFET devices.

**15.3 - 9:20 a.m.**
**Vertical Double Gate Z-RAM Technology with Remarkable Low Voltage Operation for DRAM Application,** J.-S. Kim, S.-W. Chung, T.-S.Jang, S.-H. Lee, D.-H. Son, S.-J. Chung, S.-M. Hwang, S. Banna*, S. Bhardwaj*, M. Gupta*, J. Kwon*, D. Kim*, G. Popov*, V. Gopinath*, M. van Buskirk*, S.-H. Cho, J.-S. Roh, S.-J. Hong, S.-W. Park, Hynix Semiconductor, Korea, *Innovative Silicon, USA

Vertical double gate floating body (FB) Z-RAM memory cell technology fabricated on a recess gate DRAM technology is presented. Cell operating voltage of 0.5V with comparable static retention and > 1000x improvement in dynamic retention is reported. The reported vertical double gate FB cell is the cell with the lowest operation voltage reported to date.

**15.4 - 9:45 a.m.**
**Silicon on Replacement Insulator (SRI) Floating Body Cell (FBC) Memory,** S. Kim, R. Tseng, W. Rachmady, B. Jin, U. Shah, I. Ban, U. Avci, P. Chang, Intel Corporation, USA

A 15-nm node floating body cell (FBC) memory was demonstrated utilizing silicon on replacement insulator (SRI) technology on bulk substrate. Highly selective SiGe etch and nano-scale anchors enabled the fabrication of silicon on thin replacement oxide of 12 nm. The memory characteristics show a memory signal of 7 µA and disturb retention time of 20 ms for a 51-nm gate length and 77-nm width device. This is the best FBC memory performance reported on bulk substrate.