SESSION 16 – TAPA III
Novel Devices

Thursday, June 17, 8:30 a.m.
Chairpersons: C.P. Chang, Applied Materials, Inc.
Y. Mochizuki, NEC Corporation

16.1 - 8:30 a.m.
Short-Channel Performance and Mobility Analysis of <110>- and <100>-Oriented Tri-Gate Nanowire MOSFETs with Raised Source/Drain Extensions, M. Saitoh, Y. Nakabayashi, H. Itokawa, M. Murano, I. Mizushima, K. Uchida*, T. Numata, Toshiba Corporation, *Tokyo Institute of Technology, Japan

We successfully reduced the parasitic resistance of nanowire transistors by raised S/D extensions with thin spacers (<10nm). Id variations are suppressed by spacer thinning and parasitic capacitance increase is minimal. By adopting <100> nanowire instead of <110> nanowire, Ion = 1mA/um for Ioff = 100nA/um is achieved without stress techniques. Long channel mobility was systematically studied by separating top/side channel mobility. Potentially-high mobility of <100> nFETs and <110> pFETs largely degrade due to side-surface roughness.

16.2 - 8:55 a.m.
Bistable Resistor (Biristor) – Gateless Silicon Nanowire Memory, J.-W. Han, Y.-K. Choi, KAIST, Korea

A gateless NPN Si nanowire, which has been named 'biristor' originating from bistable resistor, is presented for a high-density and high-speed memory with a standard CMOS technology. A hysteric I-V characteristic is utilized for the data storage, exhibiting a write and read time of less than 2nsec, a sensing current window of 0.23mA, and a hold retention time of 200msec. The biristor is free of cyclic endurance/reliability problem induced by hot-carrier injection due to the gateless structure.

16.3 - 9:20 a.m.
Highly Reliable Vertical NAND Technology with Biconcave Shaped Storage Layer and Leakage Controllable Offset Structure, W. Cho, S. Shim, J. Jang, H. Kim, J. Choi, C. Chung, H.-S. Cho, B.-K. You, B.-K. Son, K.-S. Kim, J.-J. Shin, C.-M. Park, J.-S. Lim, K.-H. Kim, D.-W. Chung, J.-Y. Lim, H.-C. Moon, S.-M. Huang, H.-S. Lim, Samsung Electronis Co.LTD, Korea

We have successfully demonstrated high performance 3-D cell structure for NAND flash memory. Low resistance damascened metal gate structure is achieved by the novel tungsten fill process. In addition, highly suppressed program disturbance is achieved by the proper the offset and implant conditions of SSL transistor. The proposed TCAT flash technology is very promising candidate for future NAND flash with high performance and reliability.

16.4 - 9:45 a.m.
Mobility Enhancement over Universal Mobility in (100) Silicon Nanowire Gate-All-Around MOSFETs with Width and Height of Less Than 10nm Range, J. Chen, T. Saraya, T. Hiramoto, University of Tokyo, Japan

Systematic study has been performed on mobility in sub-10nm GAA Si NW FETs on (100) SOI. The minimum NW height/width is shrunk to 4nm/5nm. For the first time, higher hole mobility than universal mobility is experimentally observed in 9nm-wide NW and even in 5nm-wide NW, demonstrating great advantage of NW pFETs, while electron mobility degradation is minimized in NW nFET. In addition, it is found that further mobility enhancements can be obtained in NWs by strain engineering. Underlying physical mechanisms are discussed.